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Design and Hardware Implementation Of 128-bit Vedic Multiplier

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Abstract: *In this paper multiplier architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, high speed applications. It is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics, Urdhva Tiryakbhyam Sutra generating all partial products and their sums in one step. The design basic block which are adders are designed in a generic way so N-bit multiplier design can be done using the designed architecture [8].The design implementation is done using VHDL (Hardware Description Language). The design code is tested using Modelsim-Altera 10.1b Simulator. The code is synthesized in Xilinx ISE 12.1 using: Xilinx, Family: Spartan XC3s1400an-4fgg676 device, Speed Grade: -4.The combinational delay of the 128×128 Vedic multiplier is found to be 38.907ns*

Keywords: *high speed multiplier, vedic mathematics, vhd, generic adder*

1. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication operations are among some of the frequently used functions currently implemented in many Digital Signal Processing applications such as convolution, Fast Fourier Transform, filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. One of the key arithmetic operations in DSP applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications .In this paper Urdhva Tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This is shown to be very similar to the popular array multiplier architecture. This paper presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is the general multiplication formula applicable to all cases of multiplication. The tools Modelsim-Altera10.1b have been used. for simulation. XILINX ISE 12.1 has been used for synthesis and verification. The Vedic multiplication technique is based on one of the 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1].

2. VEDIC MATHEMATICS

2.1 Ancient Vedic Mathematics

Ancient Indian mathematics is called as Vedic Mathematics [1]. Vedic mathematics from Vedas was first proposed by Sri Bharati Krishna Tirtha, after his survey on Vedas.

Vedic mathematics reduces the complexity in calculations that exist in conventional mathematics. The original sutras were given in Sanskrit language but here we are mentioning the most literal meaning of Sanskrit names in English.

These 16 Sutras are:-

1 By one more than the previous one
2 All from 9 and the last from 10
3 Vertically and crosswise
4 Transpose and adjust
5 When the sum is the same that sum is zero
6 If one is in ratio, the other is zero
7 By addition and by subtraction
8 By the completion or non-completion
9 Differences and Similarities
10 Whatever the extent of its deficiency
11 Part and Whole
12 The remainders by the last digit
13 The ultimate and twice the penultimate
14 By one less than the previous one
15 The product of the sum is equal to the sum of the product
16 The factors of the sum is equal to the sum of the factors

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From the sixteen sutras available in Vedic mathematics, among them only two sutras are applicable for multiplication operation. They are Urdhva Triyakbhyam Sutra (literally means vertically and cross wise) and Nikhilam Sutra (literally means all from 9 and last from 10)[2].Vedic Mathematics provides some effective algorithms which can be applied to various application fields of engineering. Out of these algorithms former proves to be a faster algorithm and applicable in all cases so it is discussed below.

2.2 Urdhva Tiryakbhyam Sutra

The given Vedic multiplier based on the Vedic multiplication formulae (Sutra). This Sutra has been traditionally used for the multiplication of two numbers. In this design, we have applied the same ideas to make the idea implemented in digital hardware [7]. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It means "Vertically and crosswise". The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be as zero. The algorithmic diagram for multiplication of two 4-bit numbers is as shown in Figure 1.

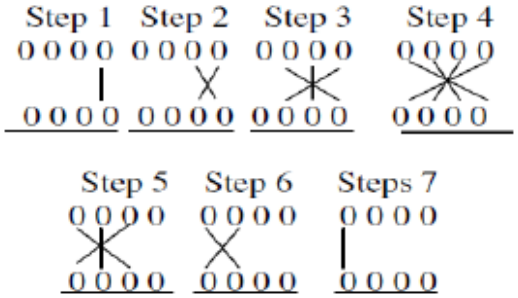

Figure 1 Algorithmic diagram for multiplication of two 4-bit numbers.

3. ARCHITECTURE OF VEDIC MULTIPLIERS

The hardware architecture of 2×2, 4×4, 128×128 bit Vedic multiplier (VM) modules are displayed in the below sections. In 2×2 bit multiplier, the multiplicand has 2 bits each and the result of multiplication is of 4 bits [5]. So in input the range of inputs goes from (00) to (11) and output lies in the set of (0000, 0001, 0010, 0011, 0100, 0110, 1001). By using Urdhva Tiryakbhyam, the multiplication takes place as illustrated in Figure. 2. Here multiplicands are a0, a1 and b0, b1. The output can be of four digits, say Q3Q2Q1Q0. As per basic method of multiplication, result is obtained after getting partial product and doing addition. The first step in the multiplication is vertical multiplication of LSB of both multiplicands, and then in the second step, that is crosswise multiplication and addition of the partial products. Then Step 3 involves vertical multiplication of MSB of the multiplicands and addition with the carry propagated from Step 2.

Multiplier	= a1	a0	
Multiplicand =	b1	b0	
		a1b0	a0b0
	a1b1	a0b1	
Q3	Q2	Q1	Q0

Figure 2: Algorithm for 2×2 multiplier

Product: Q0: a0b0
Q1: (a1b0) xor (a0b1) **(1)**
Q2: (a1b1) xor (a1b0 and a0b1) **(2)**
Q3: (a1b1and a1b0 and a0b1) **(3)**

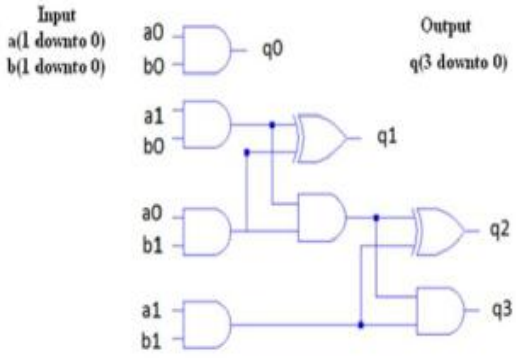

Figure 3: Hardware realization of 2×2 multiplier

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a. Generic Adder Block

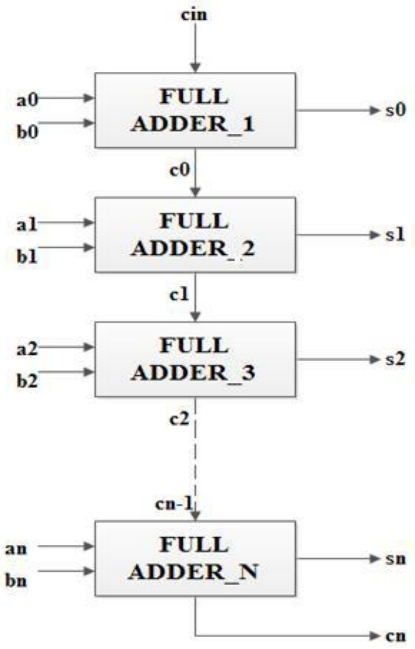

Figure 4: Hardware Realization of Generic Adder

The above shown Figure. 4 is an N bit generic adder. Here we are using ripple carry adder where initially the carry to the first block is zero by default. The carry generated to the first block is applied to the second block and carry generated to second block is applied to the next one and this process is repeated up to the N times. The Boolean function of a generic N bit ripple carry adder can be written as:

For addition

$Sum(i) = x(i)\ XOR\ y(i)\ XOR\ c(i-1)\ ,\ 0 \le i \le N-1$ **(4)**

Where i represent the current ith value and the range of i is between zero (0) to N-1.The result of this calculation is saved in ith value of sum(i).Each 1-bit adder in above Figure. 4 is described by above mentioned formulas.

For carry generation:

$C(i) = x(i)y(i) + x(i)c(i-1) + y(i)c(i-1)\ ,\ 0 \le i \le N-1$ **(5)**

$Cout = c(N-1)$ and $c(-1) = Cin$ **(6)**

Where i represent the current ith value and the range of i is between zero (0) to N-1.The result of this calculation is saved in ith value of sum(i). Each 1-bit carry generated in above Figure.4. is described by above mentioned formulae.

4× 4 Vedic Multiplier:

The 4x4 Multiplier is made by using 4, 2×2 multiplier sub blocks[4]. Here, the multiplicands are having the bit size of (n=4) whereas, the result is of 8 bit in size. The input is broken in to smaller groups of size of n/2 = 2, for both inputs, that is a and b. These newly formed groups of 2 bits are given as input to 2×2 multiplier block and the result produced 4 bits, which are the output produced from 2×2 multiplier block are sent for addition to an addition tree.

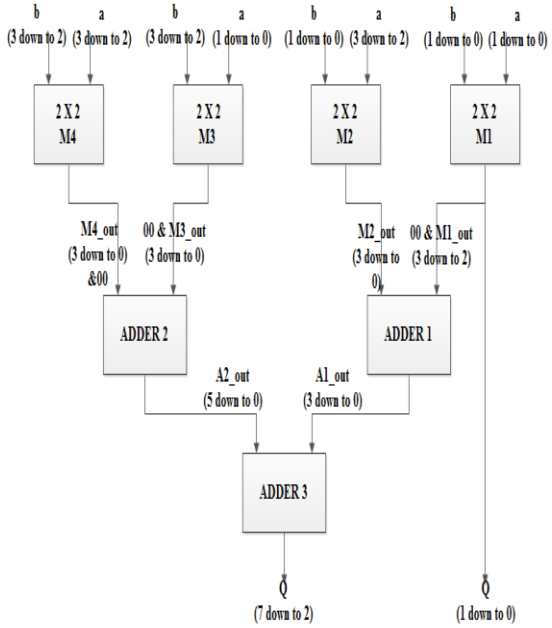

Figure 5: Hardware realization of 4×4 multiplier

With these 4×4 multiplier blocks we can design 128×128bit multiplier by structural modeling as we have already developed the generic adder.

For the ease of reading the figure6 lets take

Y=00000000000000000000000000000000000000000000000000000000000000000000

Figure 6. Shows the hardware realization diagram of an 128×128 multiplier.

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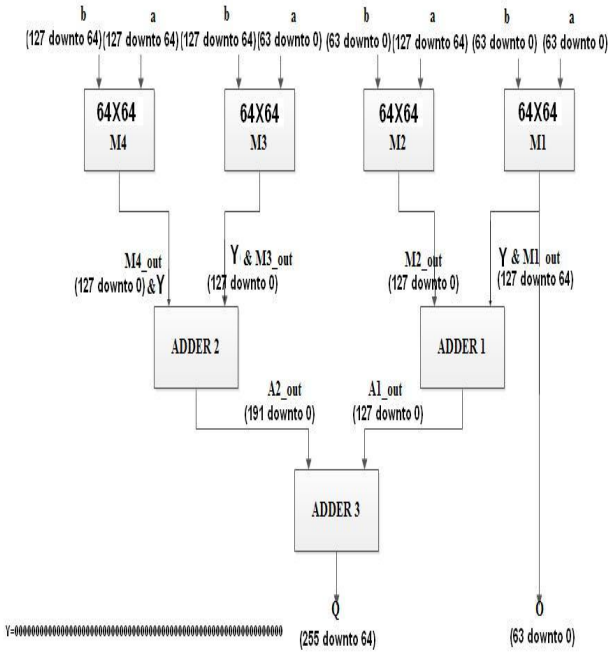

Figure 6: Hardware realization of 128×128 multiplier

4. SIMULATION OF VEDIC MULTIPLIER

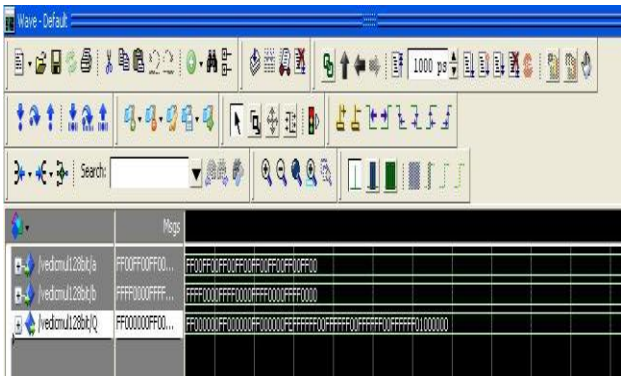

Figure 7: Simulation result of 128×128 multiplier

A= FF00 FF00 FF00 FF00 FF00 FF00 FF00 FF00

B= FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000

Q(output)= FF00 0000 FF00 0000 FF00 0000 FEFF FFFF 00FF FFFF 00FF FFFF 00FF FFFF 0100 0000

(For Simulation radix is changed to hexadecimal for the ease of reading)

ISE12.1 Selected Device: XC3s1400an-4fgg676 -4

The table below shows the synthesis report data that is the device utilization summary by the design 128×128 multiplier.

Table 1: Comparisons of Vedic & Conventional Multipliers

Multiplier	Slices Required	4 i/p LUTs	Combinational Delay
Conventional	8471	16922	41.20 ns
Vedic	5199	10248	38.907 ns

5. CONCLUSION

We can see that Vedic Multiplier is fast and as well as area efficient than the conventional multipliers. Therefore for large bit multiplication operations like DSP, it is advisable to use Vedic Multipliers

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