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WINGS TO YOUR THOUGHTS.....

CODING OF AMBA APB 2.0 PROTOCOL USING IF & ELSE STATEMENT

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Abstract*: The current electronic field is now based on VLSI .so it is very important for the designer to work on the development of chip. Many languages such as VHDL, VERILOG are mostly used by the designer.so to fulfill the need of designing and to help designer to make a compact chip I have written the coding for AMBA APB2.0 protocol. This will definitely help to work on the better performance of the bus. In my report I have provided a different coding for amba apb2.0 protocol using if &else statement. There are different method used by different designer to do the coding and by my report they will get a new way to achieve there requirement. In vlsi field it is very important to have option with the designer because there are different requirement provides the digital designer with a way of describing a system attached digital range levels of abstraction, and at the same time providing access to the tools of computer-aided design to assist in design process, which needs to be fulfilled provided by the user or the company who have requested for the design. In my work I had tried to provide a better and simple method to the designer for their design. I have chosen VERILOG hardware description language because it is mostly used by the designer nowadays and this language is widely used in industries.*

Keywords: *ambaapb, Veriloghdl, microcontroller, designing.*

1. INTRODUCTION

Verilog HDL is a Hardware Description Language (HDL).A Hardware Description Language is a language used to describe a digital system, for example, a computer or a component of a computer. One may describe a digital system at several levels. For example, an HDL might describe the layout of the wires, resistors and transistors on an Integrated Circuit (IC) chip, i. e., the switch level. Or, it might describe the logical gates and flip flops in a digital system, i. e., the gate level. An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL). Verilog supports all of these levels. However, this handout focuses on only the portions of Verilog which support the RTL level. Digital systems are very complex. At its most detailed level, this may consist of millions of elements, i.e transistors or logic gates. Thus, for digital systems larger, gate-level design is dead. For lots of decades, logic schematics served to be the lingua franca of logic design, but this is nothing more. Today, hardware complexity has grown to such an extent that a design schematic with logic gates is almost useless, since it can only display network connectivity and functionality design. Since 1970, engineers and electrical engineers have moved to hardware description languages (HDL). The most important modern HDL used in industry are Verilog and VHDL. Verilog is the top most HDL which is used by over 10,000 designers of these hardware vendors such as Sun Microsystems, Apple Computers and the Motorola industrial designers like Verilog as works[1]. The Verilog language provides the digital designer with a way of describing a system attached digital range levels of abstraction, and at the same time providing access to the tools of computer-aided design to assist in the design process in these levels. Verilog also allows hardware designers to express their design with behavioral constructs, deterring the Details of the implementation of a subsequent step in the design layout. An abstract representation also helps the designer to explore architectural alternatives through simulations and detect design bottlenecks before detailed design. Although the behavioral level of Verilog is a high level description of a digital system, is still a precise notation. Computer-aided design tools, i. e., programs, there is what is "compiled" Verilog programs level notation circuit consisting of logic gates and flip flops. Then you can go to the lab and wire logic circuits and have a working system. And, other tools can "compile" programs in Verilog notation to a description of the integrated circuit masks for very large scale integration (VLSI). Therefore, with appropriate automated tools, you can easily create a description of a VLSI design in Verilog and can send the VLSI description via email to a silicon foundry in California and can receive the integrated chip in a couple of weeks the way of snail mail.[8] Verilog also allows the designer for a specific design of the logic gate level using door constructions and constructions level using the switching transistor. Our objective in the course is not basically create VLSI chips but using Verilog to accurately describe the functionality of any digital system, for example, a computer[5]. However, a VLSI chip in which construction designed as Verilog behavior is rather slow and will waste of chip area. The lower levels in Verilog also allow engineers to optimize the logic circuits and VLSI designs to maximize speed and minimize the VLSI chip area. Verilog language describes a digital system as a set of

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modules. Each of these modules has an interface with other modules to describe how they are interconnected. Usually we put a module file, but that's not a required. The modules can be run at the same time, but usually we have a top-level module that specifies a closed system containing both test data and hardware models. The high-level module invokes instances of other modules.[9]

2. ABOUT AMBA MICROCONTROLLER

AMBA-based microcontroller typically consists of a high performance bus system backbone capable of supporting the bandwidth of external memory devices in which the CPU and a direct memory access (DMA) reside, plus an APB bus bridge to a narrower in the bandwidth peripherals are inferior. Figure shows a typical system. APB AMBA. Typically an AMBA-based microcontroller CPU, memory and other on-chip direct memory access (DMA) devices on the external memory bandwidth, capable of maintaining a high-performance system backbone bus (AMBA AHB) are. The majority of transfers are simply among the elements provides a high bandwidth interface. The addition of peripheral devices in the system is located where the lower bandwidth APB, a bridge is located in the bus. Pipelined high-bandwidth AMBA APB bus of the system as a secondary bus provides basic peripheral macrocell communication facilities. Usually such external can support:

• Registers are memory-mapped interface

• A high-bandwidth interfaces

• Programmed controls are accessed

The following points should be very much considered when reading the AMBA specification:

• Technology independence

• Electrical characteristics

• Time specification

Technology independence AMBA is a technology-independent on-chip protocol. Specification only explanation Protocol on the bus clock cycle .Electrical characteristics No information about the characteristics of electricity supplied within the AMBA This will depend entirely on the specification process Has been selected to design the technology Time specification Cycle AMBA protocol defines the behavior of the various signals. Ok Timing requirements and process technology used will depend on the frequency of Operation. AMBA protocol precise timing requirements are not defined by Time system integrator signal is given maximum flexibility in budget allocation just between various modules. AMBA APB optimized for low power consumption and reduced interface complexity is. It's for low-bandwidth peripherals such as high-bandwidth system bus used to connect Input devices
A single bus master and the transfer is to a global clock Two cycles. It may be just the boss; the system simply acts as a bridge Connected as a slave. Address and data buses can be up to 32 bits wide.

2.1 Specification

APB's operations consists of three stages, all of them are starting to grow Clock edge:
1. Waste. A transaction when it is just starting and the default position under the Way.[2]
2. Setup. A transfer is a move to the first stage of the installation. Address, Data and control signals are asserted during this phase, but may not be stable. The Stage is always a clock cycle and then move to enable operation Platform.
3. Enabled. Address, data and control signals are stable during this phase. The Phase lasts one clock cycle and then goes into the setup or disable A transfer is required or not depends on. The Advanced Peripheral Bus (APB) bus is part of the Advanced Microcontroller Architecture (AMBA) bus hierarchy and is optimized for minimum power consumption and reduced interface complexity. The AMBA APB be used to connect all peripheral devices that are low bandwidth and do not require high-performance pipelined bus interface. The most recent revision of the APB ensures that all signal transitions are related only rising edge of the clock. This improvement involves that the APB peripherals can be easily integrated into any of design flow, with the under mentioned advantages:
• The performance is improved in high frequency operation
• The performance is independent of the mark-space ratio clock
• static timing analysis is simplified by using a single clock edge
•There is no special considerations are required for automatic insertion test
• Many libraries application specific integrated circuits (ASIC) have better selection of rising edge registers
•It's easy to integrate with cycle-based simulators.
These changes in the APB also make it easier to interface to new advanced high performance bus (AHB). AMBA APB bus is part of a hierarchy and at least is optimized for power consumption and reduced interface complexity. AMBA AHB to APB is explained as one that appears as a local secondary bus Or a USB slave device. APB system bus, which provides a low-power extension AHB directly or via a USB signals. APB bus bridge handshake and handles, which appears as a slave module. From local peripheral bus control signal retiming. Defining the APB From the starting point of system bus interfaces, system diagnostics benefits And test method can be exploited. At the AMBA APB interface to any external devices which are to be used to A pipelined bus interface bandwidth and do not require high performance. The latest amendment of APB relate only to the signal transition is specified to the rising. Edge of the clock. The APB peripherals can be improved With the following benefits easily integrated into any design flow:[10]

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• Easy to obtain high frequency operation
• mark space ratio is independent of the clock
• by the use of a clock edge static timing analysis is simplified
• Any special considerations automatic testing is required for entry
• Huge Application Specific Integrated Circuit (ASIC) is better for libraries Select rising edge registers
• It gets easier integration with cycle-based simulators.

AHB to APB interface to these changes also make it easier to create new ones. Implementation of an AMBA APB bridge is usually a single AHB slave devices in a format suitable for transfer need to be changed or Asb on APB. Bridge, all address, data and control signals provides latching Slave to generate well as providing a second level of decoding signals for the selection of APB External. APB on all other modules is slaves. The following is an APB slave Interface Specification:

• When using valid address and control (unpipelined)
• no electrical activity during non-peripheral interface bus (peripheral bus is stationary When not in use)
• Time strobe time (unclocked interface) can be used with the interpretation provided by
• The use valid data (allowing glitch-free transparent latch write Execution).

Choosing the right bus for your system Before deciding on which bus or buses you should use in your system, you have to Consider the following:

• Choice of system bus
• System bus and peripheral bus
• AMBA AHB / APB when to use B or S

3. OVERVIEW OF AMBA SPECIFICATION

Advanced Bus Architecture Specification Microcontroller (AMBA) communication standard for high-performance embedded microcontroller design On Chip year.[7]

Three different nozzles are defined within the AMBA specification:

• Advanced High-performance Bus (AHB)
• advanced system bus (ASB)
• Advanced Peripheral Bus (APB).

Macro modular test and a test method provides an infrastructure for clinical use is included in the AMBA specification.[3]

Terminology

The following terms are to be used throughout this specification.

Bus cycle: A bus, a bus cycle clock period and AMBA AHB or APB protocol is a basic unit for the purpose of describing the rising edge is defined by the rising edge of change. ASB bus cycle to change a rising edge is defined by the falling edge. Bus signal is referenced to the bus clock cycle.

Bus transfer: An AMBA AHB bus transfer APB or may take one or more bus cycle operation of a data object, the read or write. Bus transfer ends with a complete response from the slave addressed. Asb transfer size supported by AMBA byte (8 bits), halfword (16-bit) and word (32-bit) are included. AMBA AHB additional 64-bit and 128-bit wide data transfers, including transfers supports. An AMBA APB bus transfer is a read or a data object always requires two Choice of system bus AMBA AHB and APB. Both are available for use as main system bus. Usually The system bus interface module provided by the system will depend on the choice of Necessary. AHB is recommended for all new designs, it offers a higher bandwidth, not only because Solution, but also results in a single clock edge protocol Used during a typical ASIC design, seamless integration with automation tools Development.

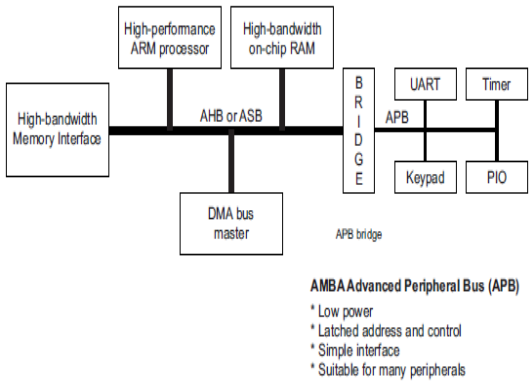

Figure 1: The typical AMBA system[2]

3.1 System bus and peripheral bus

A fully functional AHB or all the external devices such as USB module is possible to build, but can be Not always desirable:

• Increased peripheral bus with a large number of macrocells in the design Load can increase the power dissipation and performance of sacrifice.

• Timing analysis is required, just slower element will limit Maximum performance?

• Several simple peripheral macrocells latched address and control signals as needed benefit from the higher bandwidth pipelined opposed to macrocells Signal.

• Many peripheral functions required simply conveys a strobe selection macrocell without the need to select, just read and write operations / Transmit high-frequency clock signal to each peripheral. AMBA APB peripherals power is low. AMBA APB interface to work medium peripheral and less complexity for minimum power consumption is optimized. APB bus system in conjunction with the release of either can be used.[6]

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4. DESIGN PERSPECTIVE & METHODOLOGY

Verilog hardware designers in industry and education used by the two main hardware description languages (HDL) are one. VHDL is the other. Currently the industry is divided on which is better. VHDL Verilog learn and easy to use many of the sounds. Like a hardware designer says, "VHDL I hope the competition uses." The VHDL Verilog was confirmed in the year 1995 and in the year 1987 as an IEEE standard. Verilog is similar to C and C + + language learn in college is most preferred by electrical and computer engineers. VHDL is like ADA and the engineers have no experience with Ada. Now Verilog Gateway Design System Corporation, Cadence Design Systems, Systems Division Inc. "was developed in the year 1985 by a part of. By May 1990, Verilog Open International (OVI) with the formation, Verilog HDL pool was a proprietary language. Cadence Verilog HDL language users adopt other software and service companies and Verilog design tools to develop consistent wanted, she realized. Such architectural or transaction level, as well as very large scale integration (VLSI) integrated, leading to lower levels of performance (ie, door and switching levels) as: Verilog HDL designer at a higher level of abstraction To describe the hardware design allows circuit (IC) chip design and manufacturing. HDL Designer must first be committed to building is primarily designed to emulate. This material does not cover all Verilog HDL target architecture and behavior focuses on using Verilog HDL levels. Brochure design, register transfer level (RTL) emphasizes.[4] Hardware description language in late 1990 Verilog (HDL) synthesis However simulations and became the language used to describe hardware, standardized by the IEEE first two volumes (1364-1995 and 1364-2001) to test only the individual buildings. The goal was not for verification engineers. Measure designed as cross-language verification capabilities, OpenVera hardware verification language as commercial and E (HVL) was created. The two languages, one for verification and to have a design and was very painful. The productivity crisis (with a similar design on the side) resulted in the establishment of Accellera, EDA companies and a consortium of users you want to create the next generation of Verilog. Open Vera charity formed the basis of the features of SystemVerilog HVL language.

5. CONCLUSION

The APB3 protocol for the flexibility and for the adaptability of this report has shown a general definition. APB bus protocol and their performance study AMBA3 society we describe here and verification low peripheral processor data transfer protocol design are discussed. And the error is reduced without loss of data, and the move.

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