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DESIGN AND IMPLEMENTATION OF 256 BIT CMOS MEMORY CELL AT 45NM USING CADENCE VIRTUOSO

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Abstract: *SRAM are used as a interface among the CPU and since it consumes very less power it exchange DRAM from system. Low power SRAM is very important as it uses less power and also the area is very less. In many IC SRAM is embedded for some better performance. This paper discovers the working of 256 bit SRAM at 45nm technology the help of 6T cell. Here in this read access time and write access time are also calculated. In this paper designs of many components are there like sense amplifier, decoders, pre charge, write circuit and 16 × 16 cell has been designed implemented and analyzed by using Cadence Virtuoso.*

Keywords: *6T SRAM, Cadence Virtuoso 45nm, read and writes timing, low power consumption.*

1. INTRODUCTION

We have seen from twentieth century to present semiconductor field is Emerging as the useful and dominating sector. Nowadays industries are using electronic circuits. In fact our daily life greatly depends on microelectronics circuits. As we also know that SRAM is the important as it covers large area in the chip surface and SoC design i.e. almost 70% of the Cell area is consumed by SRAM memory cell. Over three decades scaling of CMOS technology is been a primary issue to the industry which helps in smaller and faster operation. As nowadays transistors which are formed today occupy less than 1% of area and are 20% faster than the other chips. The array which is designed works on the low power and gives the feasible output. The array is made of 256 bit with the help of 6T cells by the help of Cadence virtuoso schematic and layout editor. Also many other circuits also been designed such as sense amplifier, pre charge circuit, write circuit, row and column decoder. So the SRAM is been constructed by low power, high speed and less accessible time.

2. LITERATURE REVIEW

We have seen the overall SRAM architecture in the figure. It involve row and column decoder, sense amplifier, write circuit and memory cell array. We know that if number of data lines is n and number of address lines are m then then the memory so found will be 2^{m+n} . In this structure we have seen the column signifies bit and bit bar line for loading and receiving data and row is to signify particular word lines and helps in selecting particular cell. Here for fast read and write operation we use different sense amplifier and write circuit. In this way it operates in fast speed and better result [1].

2.1 Generalized SRAM Structure

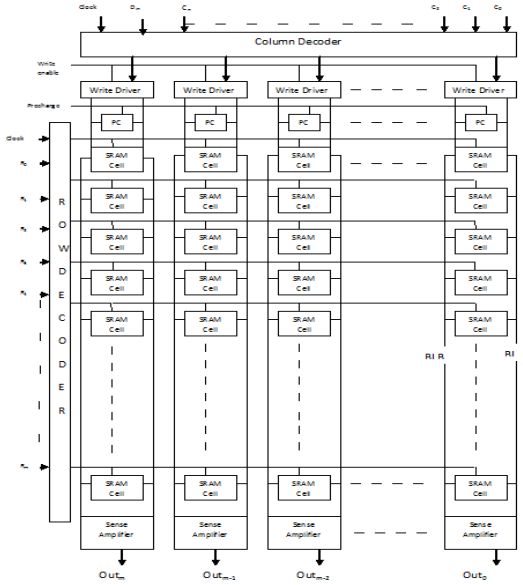

Figure 1: Overall structure

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3. DESIGN METHOLOGY

3.1 Memory cell

Memory cell is an important part of the memory cell as it loads 1 bit of value it itself. A 6T cell is most important for its robustness its low power and its low voltage operation. A SRAM uses two cross coupled invertor and used for storage of 1 bit data. In figure 2 we see a 6T invertor in which Q3 and Q4 are pMOS transistor and Q1 and Q2 are nMOS and are driver circuit. Q5 and Q6 are access transistor with the help of which cell is been accessed by the help of word line [2]. They help in transfer of data for read and write operation. Small voltage scaling are also been detected. In this the cell requires 1V of input voltage. So in 45nm the supply voltage is low so the power consumption is also low [1].

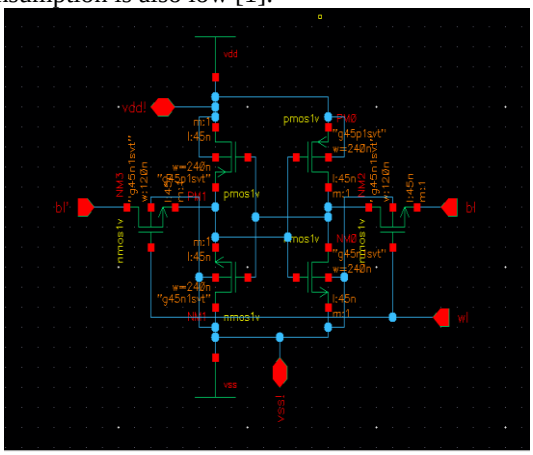

Figure 2: SRAM 6T Cell

3.2 Pre charge circuit

Pre charge is one of the most important parts of the SRAM design. The main function of pre charge is to charge the bit and bit bar line to the VDD. Pre charge makes sure that the bit line stay charged all the time except for the read and write time. It is composed of three pMOS circuit. M1 and M2 are used for pre charging and the middle one is for equalizing.

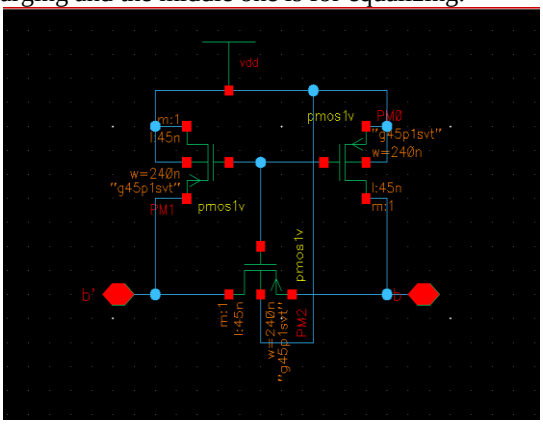

Figure 3: Pre Charge Circuit

3.3 Sense Amplifier

Sense amplifier plays a vital role in SRAM design. The choice of sense amplifier helps in robustness in read operation. The most important function of sense amplifier is to amplify the small differential voltage in the bit and bit bar line by a read access cell to the digital output signal and reducing the time foe read operation. Bit lines have large amount of capacitance as they are of metal and many access transistors are also connected to the bit line so due to which substantial amount of time is required for bit lines to discharge. So hence with small difference in the voltage the full output is out. It consists of two cross coupled stage [3]. The cross coupled makes sure a full amplification of input signal. Also a nMOS is connected to the bottom of the stage for the data enable port. Since the circuit which we have drawn is asynchronous so hence no clock is applied to it. Schematic is shown in the figure below.

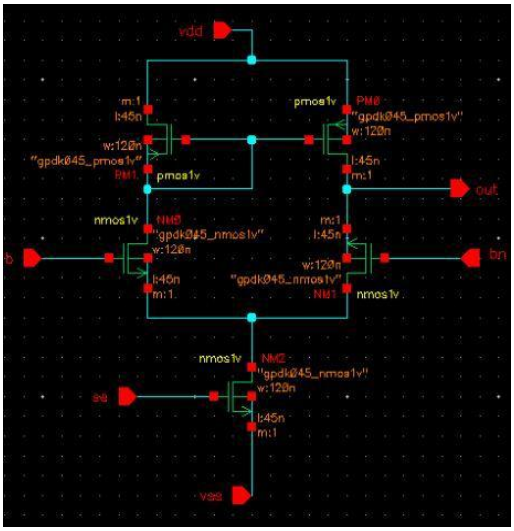

Figure 4: Sense amplifier

3.4 Decoder

The decoder is important part of the SRAM circuit. There are two type of decoder which are generally used those are row and column decoder. Address decoder is used to decode the input address and is used to enable the word line. The two type of decoder used is made of NAND gate. Row decoder is used to pick up particular word line by setting the voltage high and column decoder is used to select a particular column. Here we opt for 2 to 4 decoder for column decoder. In this we enter two values and we get four output. For row decoder we used pre decoder system in which we used two 2 to 4 decoders and with their output we applied it to two input NAND gates according to the logic and then we get the 16 outputs which we applied to the word lines [3].

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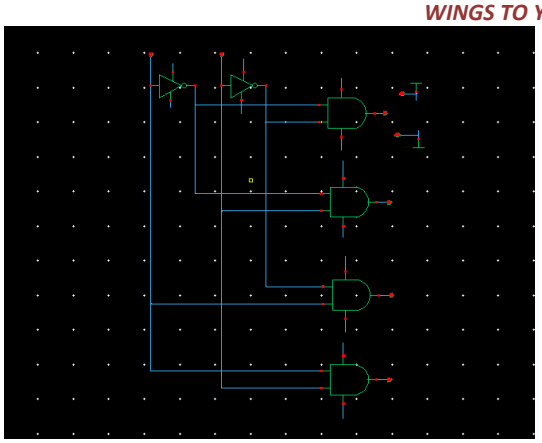

Figure 5: Decoder (2 to 4)

3.5 Write circuit

The main function of write circuit is to immediately discharge one of the bit lines by the help of pre charge circuit to the write margin of the SRAM cell. Generally write circuit is enabled by the write enable signal and drives the bit lines using the using full swing discharge from pre charge level to ground. Write driver uses two stacked NMOS transistors to form two pass-transistor AND gates using NMOS Q1, Q3 and Q2, Q4 transistors [4]. The two input are word line and data line which is applied to the AND gate and to the write bar output and also the input write enable and data is also applied in invertor and then to the AND gate and then we get the output to the write output. Here, we are used basic CMOS inverter and NMOS pass transistors that form our write driver circuit [1].

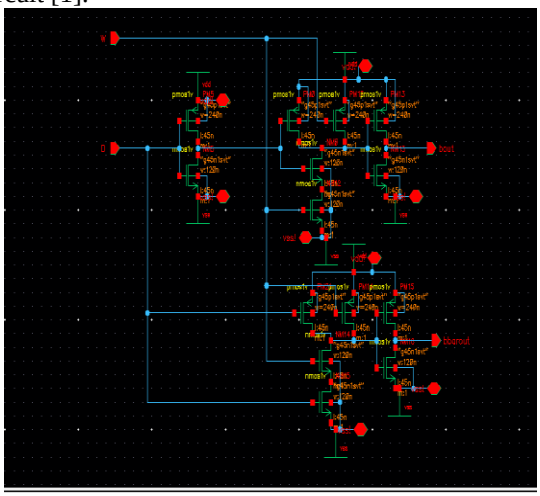

Figure 6: Write circuit

4. RESULTS

This section tells about the result analysis and the simulation which took for 16 × 16 memory array by the help of cadence virtuoso by spectre. With the aid of this we were able to find out the read and write timing of each case. Also we have derived its waveform as shown in the figure. In this case we have seen the input voltage is 1V and with help of which the total power consumed is also quite low.

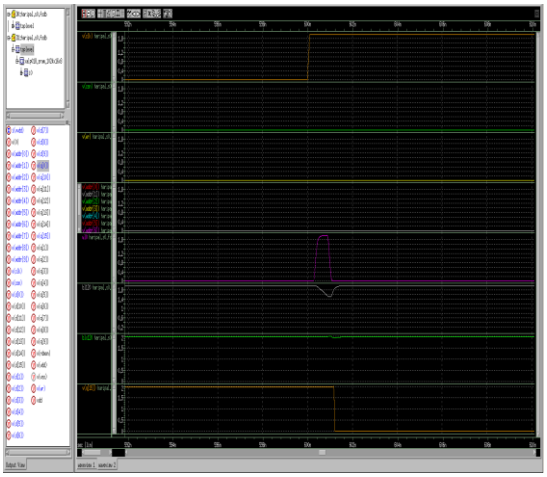

Figure 7: Write 0

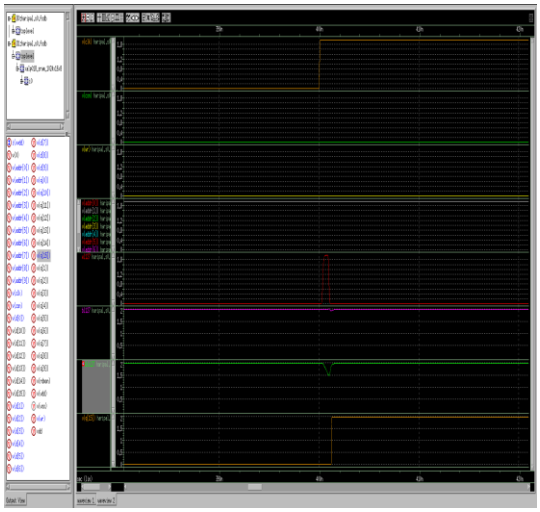

Figure 8: Write 1

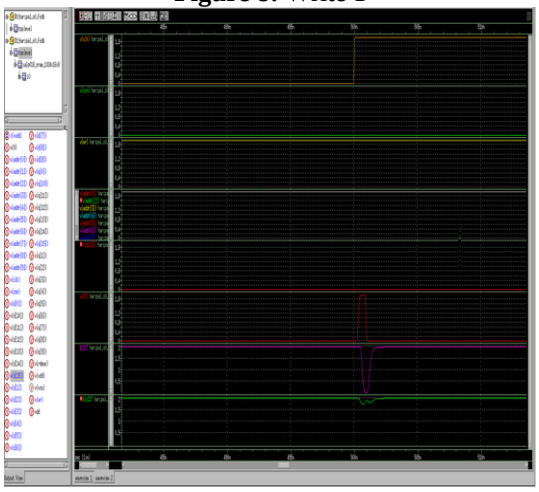

Figure 9: Read 0

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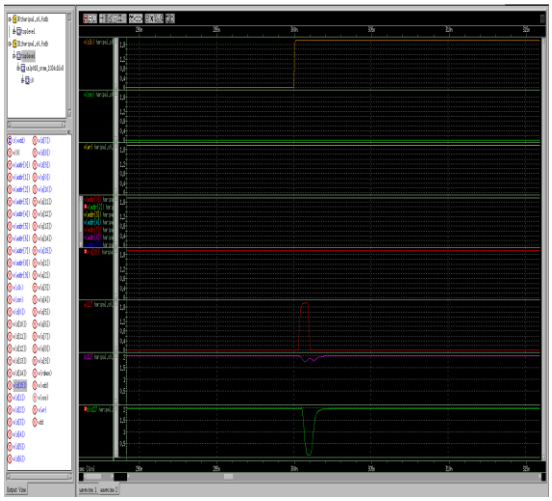

Figure 10: Read 1

Here after the simulation we calculated the write0, write1, read0, read1 timing with the help of cadence spectre which was 120ps, 0.74ns, 84ps, 1.04ps respectively. The proposed work is performed under the analog voltage of 1V and consumes the total power of 1.508 mV. The total area consumed in this by a 6T cell is 12.35 mm^2. The whole SRAM is designed and implemented by Cadence virtuoso version 6.1.1 gpdk045.

5. CONCLUSION

We have designed the new 256 bit memory cell in which we have designed the read and write operation. Hence according to this project corresponding read and write operation have been noted. It is a four bit input output memory cell i.e. in the input side four input were given and four output were received. So we have successfully designed its bit cell that means a 6T SRAM in which 1 bit of is been stored and also placed accordingly to make an array of 256 cells. We also checked for the DRC in every step of formation of memory so that no sign of errors should occur.

6. ADVANTAGES

We have also seen that the technology is also getting smaller and smaller and here we have used the 45 nm technology. In this way there are many significant advantages of this technology:

- It helps in reducing the size of the VLSI chip.
- It helps in improving the speed of the chip.
- In this the total power consumption is very low.
- Also low voltage is used.
- Increase the accuracy.

So these are the advantages of using low nm technologies compared to 90 and 180nm.

8. FUTURE WORK

The future work of this project is mostly going to be in scaling technology. That is since we have used 45nm technology which is been brought from 180nm then 90nm then to 65nm. Hence the upcoming technologies are going to less than 45nm. Nowadays 22nm and 14nm have been proposed to work on the chip design from the foundry. So therefore scaling down will be continued to the coming generation.

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