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DESIGN OF A LOW POWER 2T SRAM CELL USING TRANSMISSION GATE

[1]Digvijay Singh Deora, [2]Ghanshyam

[1]Research Scholar, Department of ECE,
GyanVihar School of Engineering and Technology
(SGVU), Jaipur, Rajasthan, India
gofordigvijay@gmail.com
[2] Assistant Professor, Department of ECE,
GyanVihar School of Engineering and Technology
(SGVU), Jaipur, Rajasthan, India
ghanu.4us@gmail.com

ABSTRACT*: The power consumption and speed of SRAMs are important issues that have lead to multiple designs with the purpose of minimizing the power consumption. The less power a circuit consumes, more effective is the performance of a device. Use of transmission gates in place of pass transistors in 4T SRAM has been proposed in this thesis work to reduce the power consumption in the SRAM cell. By simulating the conventional 4T SRAM cell and the proposed cell circuit on Tanner T-spice software we will analyze the power consumption in both circuits.*

Keywords: *4T SRAM, Transmission gate, simulation, Tanner T-spice.*

1. INTRODUCTION

The basic requirement of a digital circuit is that it satisfies the designing goals and to provide a good quality product. The designing goals deal with the function of the circuit and the quality of the circuit is governed by optimizing the parameters of area, performance and power consumption. An efficient electronic circuit is one which fulfils these requirements.

The increasing market of mobile devices and battery operated portable electronic systems has led to innovative developments in the low power design during the recent years. Demands for chips that consume smallest possible amount of power and satisfy equally demanding goals of high chip density and high throughput has rapidly increased.[1]

Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems.Memory elements are the biggest source of power dissipation in any digital system and any digital circuit is incomplete without memories. The power consumption and speed of SRAMs are important issue that has lead to multiple designs with the purpose of minimizing the power consumption. [2]

Every digital system now a days is strongly dependent on the memory .we can also say that no digital system now a days can be built without memory. It is also the heart of any microprocessor and that is why most of the research in low power design is going to design the memory.Many different methodologies are used for the fabrication of a SRAM memory cell.These methods are based upon improving the design quality of the SRAM cell in terms of area,performance and power consumption.

The basic motive of this research work is to analyze the SRAM memory cell which will consume lesser power as compared to the 4T SRAM cell.In the forthcoming sections we will first discuss the 4T SRAM cell and then the proposed work in next and at last result and conclusion.

2. LITERATURE REVIEW

4T SRAM Cell:

The basic building block of a SRAM is the SRAM memory cell which holds the data to be stored in the memory. SRAM is formed from an array of many such memory cell. The basic circuit consist of asimple latch circuit (two cross coupled inverters) with two stable operating points.To access the data contained in the memory cell via the bit line, a switch is used which is controlled by the word line.[3] Fig. 1 shows a basic 4T SRAM cell. It consists of 4 Nmos transistors and 2 resistors as its building blocks.

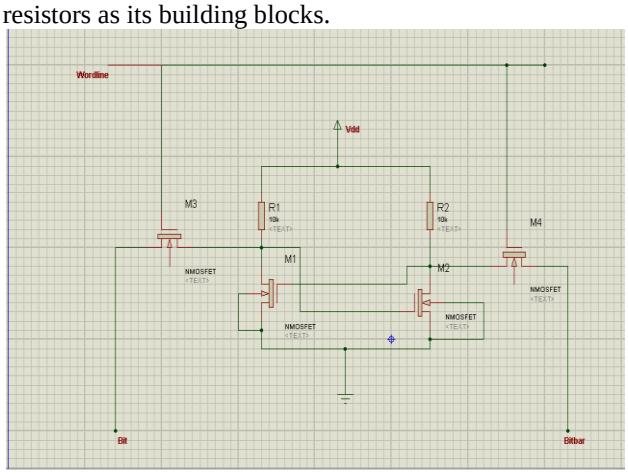

Figure 1: Schematic of 4T SRAM cell.

Two transistors M3 and M4 act as pass transistors which connect bit lines to internal nodes of cell. Transistors M1 and M2 acts as driver transistors. The resistors R1 and R2 form the load of the cross coupled circuit.The power optimization is analyzed in three modes:

(A) Read mode:

The first step while performing read operation is precharging the bit lines to Vdd. The read operation is

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performed when the word line activates the pass transistors and thus enabling the bit lines BL and BLB to connect to internal nodes. To read '1' BL retains its charge and BLB is pulled down by transistors M2 and M4. This decrease in voltage is read by the circuit as logic 1. To read a '0', BLB retains its value and BL is pulled down by transistor M1 and M3.

(B) Write mode:
The write operation is performed in SRAM by providing the values to be written to bit lines. If we want to write '1' then BL will be given logic 1 or will be kept high and BLB will be discharged to logic 0 or kept low. When the word line is activated, the input node is written with logic high or 1. To write a 0, the BL is kept at 0 or logic low and BLB is kept at logic 1 or high. When the word line is activated, logic 0 is written to the internal node of the cell.

(C) Standby mode:
Pass transistors will disconnect from the cell bit lines when the word line is not asserted. Two cross inverters formed the two inverter which is connected back to back reinforce each other as they are disconnected from the outside world. And they will pass the data in which they have already stored in the memory cell. [3]

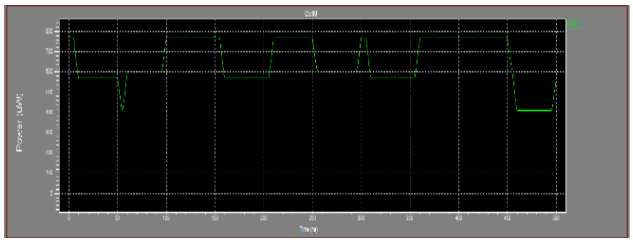

Figure 2: Power waveform of read operation.

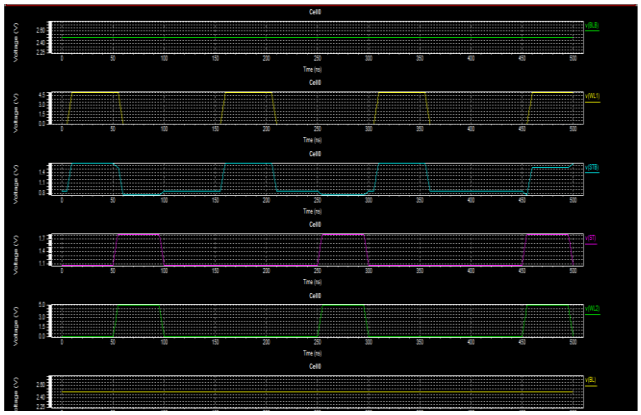

Figure 3: Voltages in read operation.

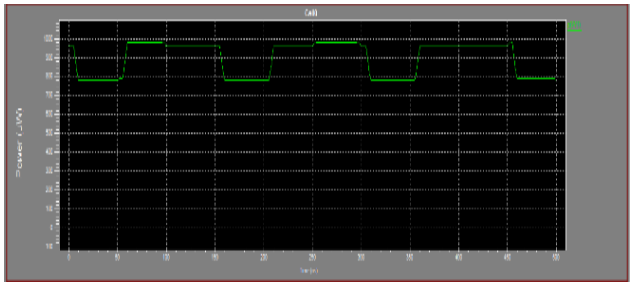

Figure 4: Power waveform in write operation.

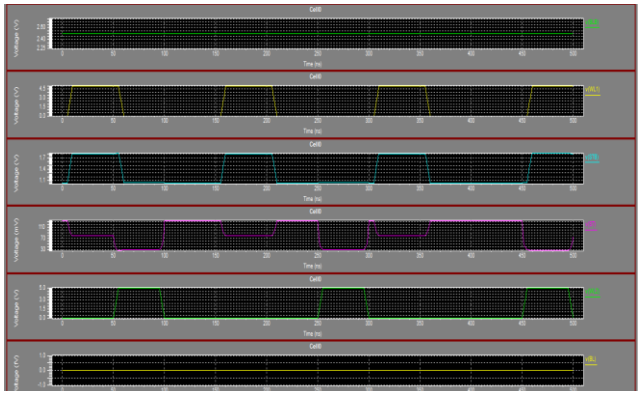

Figure 5: Voltages in write operation.

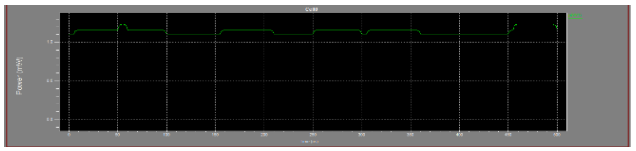

Fig 6: Power waveform of Standby mode.

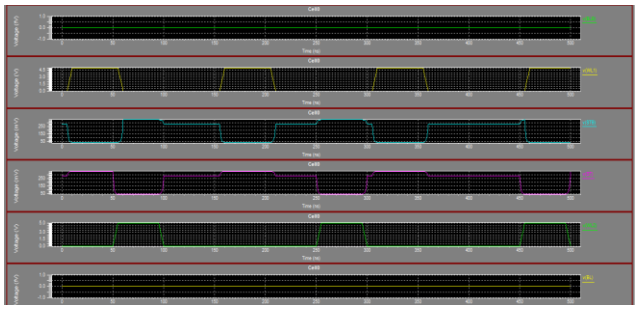

Figure 7: Voltages in Standby mode.

3. PROPOSED WORK

The proposed SRAM cell is shown in Fig. 12. The motive behind the work is to utilize the benefits of transmission gates in the SRAM cell circuit. The transmission gate circuit is effective in transferring the input voltage to the output without any attenuation. Transmission gates enable rail to rail swing. It works as a switch network which is capable of transferring the input voltage to output without threshold attenuation. [4]

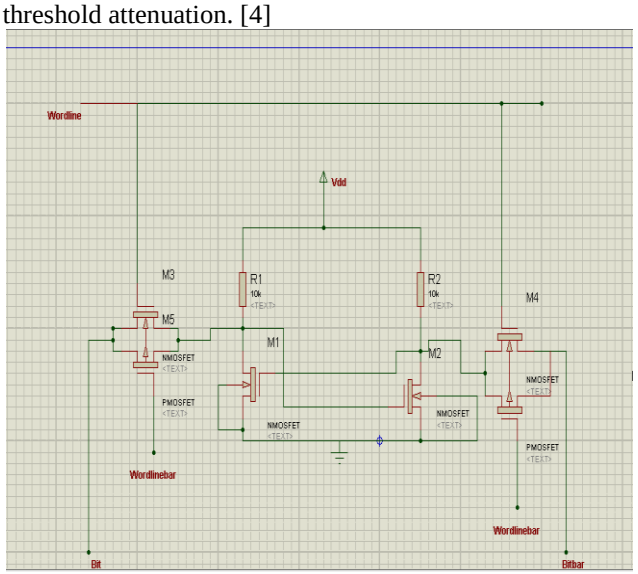

Figure 8: A 2T SRAM cell using transmission gate.

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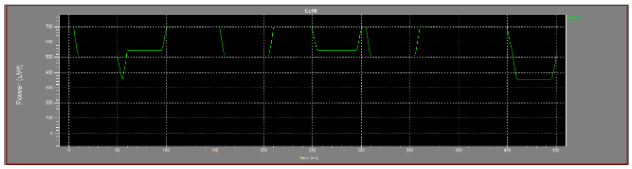

Figure 9: Power waveform of Read operation.

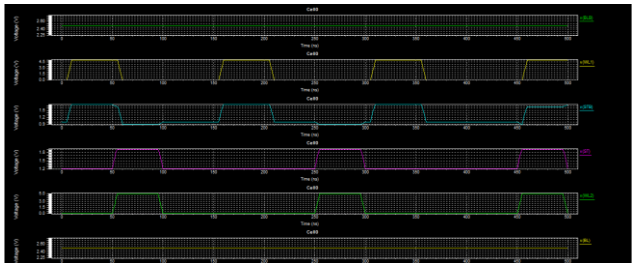

Figure 10: Voltages in Read operation.

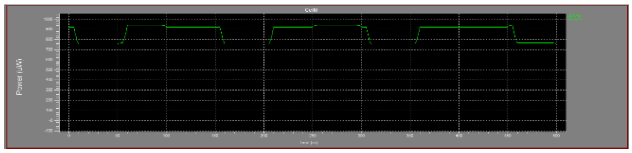

Figure 11: Power waveform of Write operation.

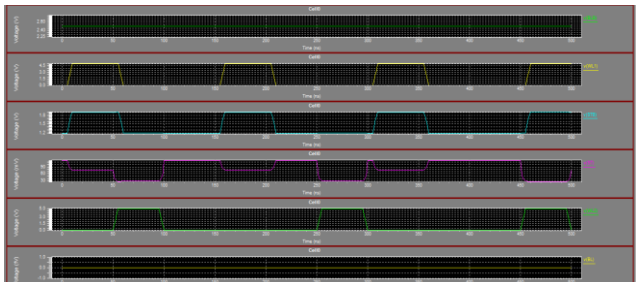

Figure 12: Voltages in write operation.

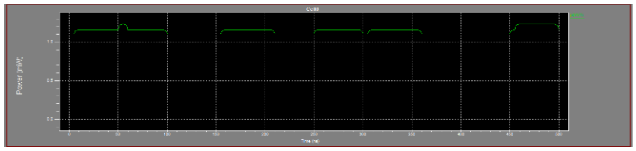

Figure 13: Power waveform of Standby mode.

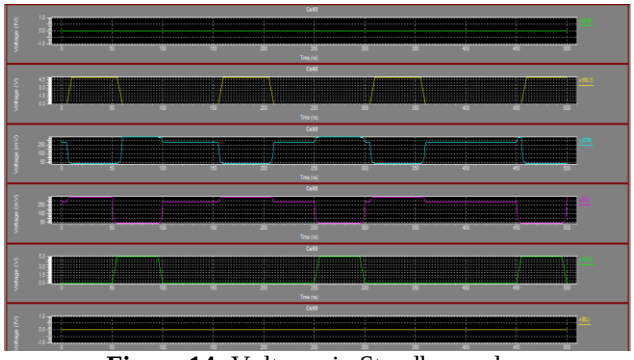

Figure 14: Voltages in Standby mode.

4. SIMULATION ANALYSIS AND RESULT

The work has been simulated in TSPICE simulator using a 250nm standard technology. The simulation conditions are summarized in Table -1.

Table – 1: Simulation Conditions.

Device Name	Parameters
Resistors	10k
PMOS & NMOS	W/L = 2.5u / 0.25u
Simulation Condition	
VDD	2.5V
BL	2.5v
WL	5v Pulse

(A)RESULTS:

We have successfully simulated the proposed work and the previous work and the results show that the proposed design is effective in reducing the power consumption in a SRAM cell. Table – 2 shows the comparison between the 4T SRAM cell and the proposed design on basis of power consumption.

Table – 2: Results.

Mode	Previous work (Average power consumption)	Proposed work (Average power consumption)	% Change
Standby Mode	1.143785e-003 w	1.143794e-003 w	Negligible
Write 1	9.167252e-004 w	8.844495e-004 w	3.52
Write 0	8.935467e-004 w	8.628285e-004 w	3.43
Read 1	6.471104e-004 w	5.813082e-004 w	10.16
Read 0	6.512008e-004 w	5.855091e-004 w	10.08

5. CONCLUSION

In this paper, we have designed a low power 2T SRAM cell using transmission gate. We have successfully analyzed the 4T SRAM cell and the proposed SRAM cell and found out that the 2T SRAM cellwith transmission gate is more efficient and consumes less power than the 4T SRAM cell.

REFERENCES

[1] Masood Qazi, Mahmut E. Sinangil, and Anantha P. Chandrakasan, "Challenges and Directions for Low-Voltage SRAM", Copublished by the IEEE CS and the IEEE CASS 0740-7475/11/$26.00 2011.

[2] Kaushik Roy, Sharat C. Prasad, "Low-Power CMOS VLSI Design", a John Wiley & Sons, 02-Feb-2009.

[3] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill Education.

[4] Sunil Kumar Ojha, P.R. Vaya, "A Novel architecture of SRAM cell for low power application", ISSN (Print): 2278-8948, Volume-2, Issue-4, 2013.