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EXPEDITIOUS RIPPLE CARRY ADDER POWERED BY BOOLEAN LOGIC

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Abstract: *- Among the known adder circuits we know that Carry Select Adder is the fastest. This work is streamlined version of the carry select adder. Logical simplification shows that we see that an OR gate and an Inverter would suffice. A multiplexer is used for selection of the output according to the logical state of the input carry. Based on this logic Expeditious CSLA (ECSLA) design has been modelled and is compared with the existing models. The Modified CSLA architecture has been developed using Binary to Excess -I converter (BEC). In this paper we propose a speed and cost effective method which substitutes a BEC using simple Boolean logic. Our analysis shows that the proposed design achieves 3-way advantages in terms of area, power and delay .Note that this is different from Sqrt CSLA from that it uses half adders near the input carry instead of full adders.*

Keywords: *Expeditious Carry Select Adder, Area-Efficient, Boolean Logic.*

1. INTRODUCTION

The fundamental operation involved in every digital system is addition. In any application these are most prominent. Applications involving them include DSP, FFT, Filters, and Brain Empowered Wireless communications (Refer: Simon haykins). In Advanced RISC processors it is required to perform additions millions of times per second. Hence it is understood that speed has its importance. The time taken by the carry to make its way from one full adder to another for selection limits the speed of the device. This is because the sum and carry for successive bits are generated only when the previous stage carry is made available.

The Carry Select Adder is used in many computational systems to ameliorate the problem posed by carry propagation delay. This is done by generate different carries for logic states '0' and'1' and then multiplexing it with previous stage carry for the required output. But CSLA suffers from the limitation of having multiple Ripple Carry Adders (RCA). The streamlined version of CSLA is to use Binary to Excess-I Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lesser area and power consumed with a hike in delay.

The theory behind the proposed design is that which replaces the BEC by Simple Boolean Logic. Here we present an expeditious version of a carry select adder by sharing the Boolean logic term. After the proposed innovation, we can get a streamlined version of the CSLA. It generates an alias sum and Carry-out signal by logically utilizing NOT and OR gate and multiplexing the value with the previous stage carry[3].

In this paper we will first analyze the already existent CSLA and BEC converters (Sections 2 and 3 respectively .In section 4 we show the usage of Boolean logic and section 5 we explain about the proposed design. Area, power and delay Results are analyzed in the section 6. Section 7 deals with conclusion.

2. ANALYSIS OF REGULAR CSLA

The Carry select adder uses two ripple carry adders and a 2: 1 multiplexer .The major limitation of CSLA is the large area due to the two ripple carry adders. The 16-bit Carry select adder is shown in Fig A.[7]

The 16-bit Carry Select Adder

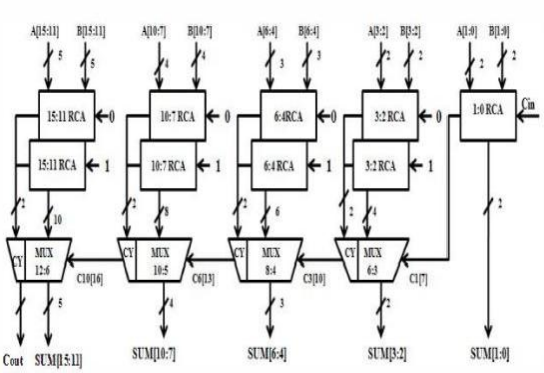

Fig: A

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It is sectioned into five groups with variable bit size RCA. From the structure of CSLA, we can reduce area and power consumption. The Cout evaluated from the previous stage is used in selection by the multiplexer.[1] Internal structure of the group 3 of regular 16-bit CSLA is shown Fig B. The number of gates used for group 3 is 87 and delay is 13 ns. The inputs to the mux are from the RCA with Cin=O and Cin=1.

Group 5 of the 16-bit Carry Select Adder

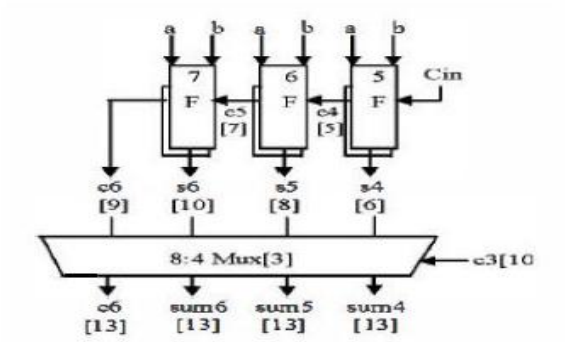

Fig: B

3. MODIFIED CSLA

It uses a single ripple carry adder with a binary excess one converter which substitutes the other RCA which would otherwise be required. To replace n-bit RCA we require n+1 BEC converters.[2] The characteristic table is shown in the table. The Boolean expressions are listed as:

Tabulation of the Boolean expressions

Binary[3:0]	Excess-1[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

X0=~B0
X1=B0 ^ B1
X2=B2 ^ (B0 & B1)
X3=B3 ^ (B0 & B1& B2).

The 16-bit CSLA is shown in the figure C. Its again sectioned into 5 groups with variable bit size of RCA and BEC. The group 3 of the modified 16-bit CSLA is shown Fig D. By manually counting the number of gates used for group 3 is 61 (full adder, half adder, multiplexer, BEC) and the delay is 16ns. The parallel RCA with Cin=1 is replaced with BEC. One input to the multiplexer goes from the RCA with Cin=O and other input from the BEC.

The 16-bit CSLA

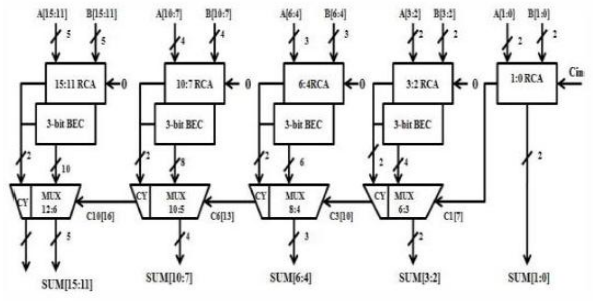

Fig C

Comparing the group 3 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA [1].

The group 3 of the modified 16-bit CSLA

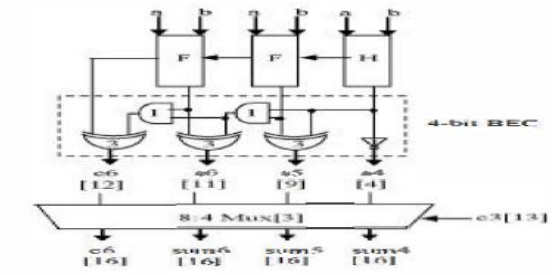

Fig: D

4. BOOLEAN LOGIC

In proposed work, an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. In this way, it save many transistor counts and achieve a low Power. Through analyzing the truth table of a single-bit full- adder, To find out that the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "I". As illustrated as two dotted circles in the truth table of Fig. E. [3] By sharing the expeditious Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig. F.

Tabulation of the Boolean Logic

C_{in}	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig: E

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Proposed Carry Select Adder Design

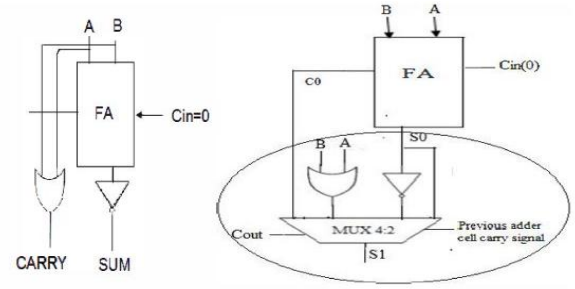

Fig: F

To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the Carry signal and summation signal pair. Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal.

As compared with the Modified Carry Select adder, the proposed CSLA is little bit faster, but the speed is nearly equal to the Regular CSLA. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder. The Proposed CSLA is Area efficient & low power, but the speed equal to the Regular CSLA.

5. THE ECSLA ARCHITECTURE

This method replaces the BEC add one circuit by Common Boolean Logic. The output waveform of full adder for carry in signal is 'I' is generate summation and carry signal by just using an INV and OR gate. It is shown in Fig G.

Modified Carry Select Adder with INV and OR gates

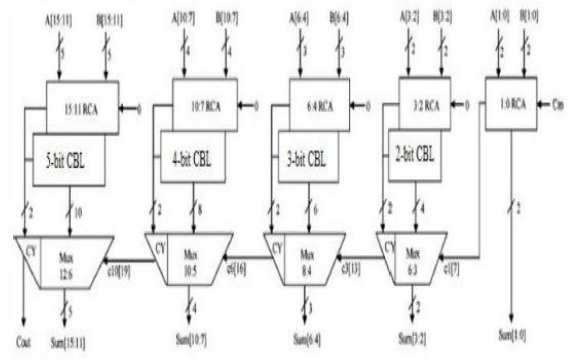

Fig G

The Summation and carry signal for FA which has Cin=l, Generate by INV and OR gate. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal .Internal structure of the group 3 of Proposed CSLA is shown Fig.H. By manually counting the number of gates used for group 3 is 36 (full adder, half adder, and multiplexer, not, or gate). One input to the mux goes from the RCA block with Cin=O and other input from the CBL.

The Proposed Carry Select Adder with the Usage of Mux

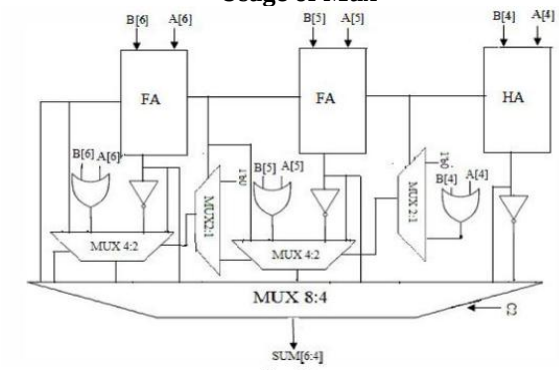

Fig: H

The Group 3 performed a three bit addition which are A [4] with B [4], A[S]with B[S] and A [6]with B[6]. This is done by I half adder (RA) and two full adder (FA). The CBL block has a 4:2 multiplexer to select the appropriate carryout and summation signal for Carry-in signal 'I'. Through 2: I multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexer and 4:2 multiplexer is the combination of 2: I multiplexer.

6. COMPARISIONS OF ADDERS

The 8-bit CSLA is done by the same structure of 16-bit CSLA except group 4 and group S. The 8th bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit CSLA is done by cascading two 16-bit CSLA and 64-bit CSLA is done by cascading two 32-bit CSLA [4]. Table 2 exhibits the delay, area and power of regular, modified and proposed CSLA Simulation is carried out using Xilinx simulation tool and Spartan 3E as the target device. The major disadvantage of modified CSLA using BEC is the increasing delay. This disadvantage is overcome in proposed architecture which reduces the delay, area and power than the regular and modified CSLA.

The results show that the proposed CSLA has higher speed when compared to regular and modified CSLA. When compared to regular and modified CSLA the proposed circuit occupies less area. In addition to realization of higher speed and lesser area as discussed above, the proposed architecture consumes less power when compared to the regular and modified CSLA.

The table containing the delay, power and area can be found in the next page.

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Comparison of Delay, area and power of proposed ECSLA and the CSLA.

Word size	Adder	Area(No. of Gate count)	Delay (ns)	Power (mw)
8-bit SQRT CSLA	**Regular** (dual RCA)	144	11.92	193
	Modified (with BEC)	132	13.69	180
	Proposed (with CBL)	111	11.15	119
16-bit SQRT CSLA	**Regular** (dual RCA)	348	16.15	315
	Modified (with BEC)	291	18.77	268
	Proposed (with CBL)	276	15.48	177
32-bit SQRT CSLA	**Regular** (dual RCA)	698	28.97	553
	Modified (with BEC)	762	34.44	448
	Proposed (with CBL)	552	26.23	321
64-bit SQRT CSLA	**Regular** (dual RCA)	1592	52.82	860
	Modified (with BEC)	1498	64.61	745
	Proposed (with CBL)	1104	47.74	555

Table: 2

7. CONCLUSION

A simple approach is proposed in this paper to reduce the area, power and delay of CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area, total power and also reduces the delay. A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. The Regular CSLA has the disadvantage of more power consumptions and occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-I converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of Boolean Logic. It would be interesting to test the design of the proposed 128-b CSLA.

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