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CLOSED LOOP CONTROLLED BRIDGELESS PFC BOOST CONVERTER FED DC DRIVE

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Abstract: *In this paper, a new control circuitry for bridgeless PFC boost converter is proposed. The bridgeless PFC boost converter utilizes a bidirectional switch and two fast diodes. The absence of an input diode bridge and presence of only one diode in the flowing-current path during each switching cycle results in less conduction loss and improved thermal management compared to existing PFC rectifiers. Here, this bridgeless boost converter circuit is analyzed and simulated with motor load. The circuit has advantages like reduced harmonics and improved power factor. Also, near unity power factor is obtained by using this bridgeless boost converter with EMI Filter. Simulation results are presented to demonstrate the feasibility of the proposed technique.*

Keywords: *Bridgeless Rectifier, Electro Magnetic Interference, Power Factor Correction, Converter Conduction Losses.*

1. INTRODUCTION

In recent years, the demand for improving power quality of the ac system has become a great concern due to the rapidly increased numbers of electronic equipment. To reduce harmonic contamination in power lines and improve the transmission efficiency, power factor correction (PFC) research became an active topic in power electronics, and significant efforts have been made on the developments of the PFC converters [1]–[4]. As a matter of fact, the PFC circuits are becoming mandatory on single-phase power supplies as more stringent power quality regulations and strict limits on the total harmonic distortion (THD) of input current are imposed [5].

The preferable type of PFC is active PFC since it makes the load behave like a pure resistor, leading to near-unity load power factor and generating negligible harmonics in the input line current [6]. Most active PFC circuits as well as switched mode power supplies in the market today comprise a front-end bridge rectifier, followed by a high-frequency dc–dc converter such as a boost, a buck–boost, a Cuk, a single-ended primary inductance converter (SEPIC), and a flyback converter. This approach is suitable for a low-to-medium power range. As the power level increases, the high conduction loss caused by the high forward voltage drop of the diode bridge begins to degrade the overall system efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes. Hence, it becomes necessary to utilize a bridge rectifier with higher current-handling capability or heat-dissipating characteristics. This increases the size and cost of the power supply, which is unacceptable for an efficient design. Another reason for high conduction losses in conventional active PFC circuits is due to the fact that during each switching cycle, there are always three power semiconductors in the flowing-current path (two slow recovery diodes plus an active switch or a fast-recovery diode). Thus, in an effort to improve the efficiency of the front-end PFC rectifiers, many power supply manufacturers and some semiconductor companies have started looking into bridgeless PFC circuit topologies. Generally, the bridgeless PFC topologies, also referred to as dual boost PFC rectifiers, may reduce the conduction loss by reducing the number of semiconductor components in the line current path. So far, a number of bridgeless PFC boost rectifier implementations and their variations have been proposed.

In this paper, a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented.

2. BRIDGELESS PFC BOOST CONVERTER

In the bridgeless PFC circuit, the boost inductor is split and located at the AC side to construct the boost structure. In this first half line cycle, MOSFET Q1 and boost diode D1, together with the boost inductor construct a boost DC/DC converter. Meanwhile, MOSFET Q2 is operating as a simple diode. The input current is controlled by the boost converter and

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following the input voltage. During the other half line cycle, circuit operation as the same way. Thus, in each half line cycle, one of the MOSFET operates as active switch and the other one operates as a diode: both the MOSFET's can be driven by the same signal. Comparing the conduction path of these two circuits, here we see that at every moment, bridgeless PFC inductor current only goes through two semiconductor devices while inductor current goes through three semiconductor devices for the conventional PFC circuit. The conventional method is shown in fig. 1(a).

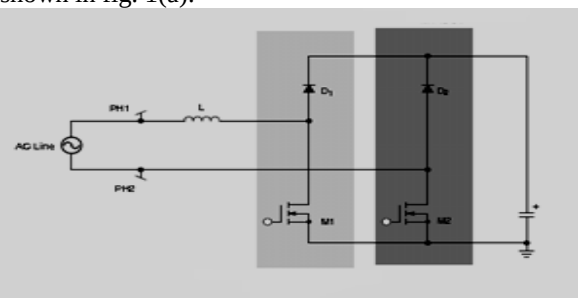

Fig -1: Bridgeless PFC circuit

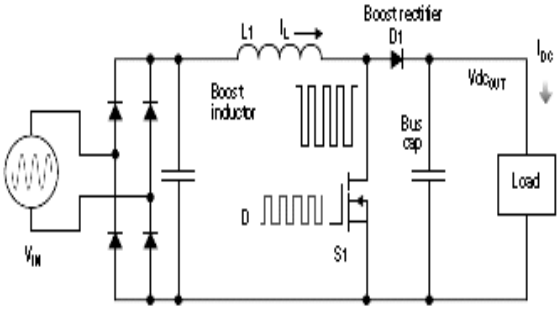

Fig -1(a): Conventional PFC circuit

Also, the bridgeless PFC uses one MOSFET body diode to replace the two slow diodes of the conventional PFC. Comparing with the conventional PFC, the bridgeless PFC not only reduces conduction loss, but also reduces the total components count.

To reduce the rectifier bridge conduction loss, different topologies have been developed. Among these topologies, the bridgeless boost doesn't require range switch, shows both the simplicity and high performance. High performance single phase AC to DC rectifier with input power factor correction is given by [7]. A new ZCS quasi-resonant unity power factor is proposed by [8]. ZVS-PWM unity power factor rectifier is given in [9]. Single phase AC to DC rectifier with input power factor correction is given in [10]. Semi resonant high power factor rectifier is presented by [11]. A power-factor controller for PWM rectifier is presented in [12]. The above literature does not deal with the modeling of closed loop controlled bridgeless PFC converter. The aim of loop controlled PFC converter.

3. CONTROL SCHEME

The objective of the control scheme of the boost converters is to regulate the power flow ensuring tight output voltage regulation as well as unity input power factor. Cascaded control structure shown in fig. 2 is the most extensively used control scheme for these converters. In this scheme, the output of voltage regulator, limited to a safe value, forms the amplitude of input reference current. This reference amplitude is then multiplied to a template of input voltage to synchronize the reference with input voltage, as required for unity power factor operation. The inductor current is forced to track its reference current using current controller, which generates appropriate gating signals for the active device(s). The various components of this control scheme are explained as follows:

3.1 Supply System

Under normal operating condition the supply system can be modeled as a sinusoidal voltage source of amplitude V_m and frequency f_s . The instantaneous voltage is given as:

$v_s(t) = V_m \sin wt$ (1)

where $w = 2 p f_s t$ electrical rad/s and t is instantaneous time. From sensed supply voltage, a template u(t) is estimated for converter topologies with ac side inductor.

$u(t) = | v_s(t) / V_m |$ (2)

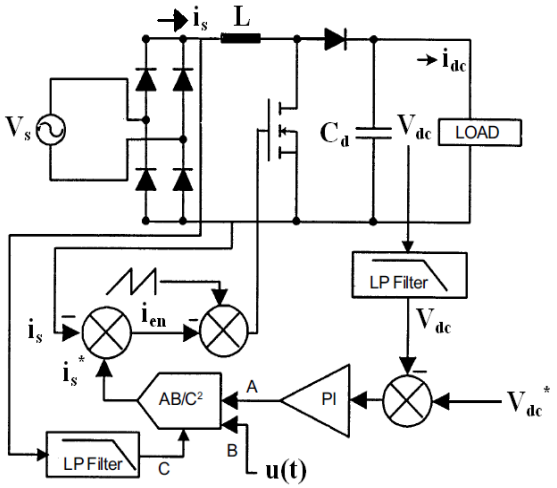

Fig -2: Control scheme of PFC Converter

3.2 DC Voltage Controller

The objective of dc voltage controller is described earlier. A proportional integral (PI) voltage controller is selected for voltage loop for tight regulation of the output voltage. The dc voltage v_{dc} is sensed and compared with set reference voltage v_{dc}*. The resulting voltage error $v_{e(n)}$ at nth sampling instant is:

$v_{e(n)} = v_{dc}^* - v_{dc(n)}$ (3)

Output of PI voltage regulator $v_{0(n)}$ at nth sampling instant is:

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$$v_{0(n)} = v_{0(n-1)} + K_p (v_{e(n)} - v_{e(n-1)}) + K_i v_{e(n)} \quad (4)$$

where K_p and K_i are the proportional and integral gain constants. $v_{e(n-1)}$ is the error at the (n-1)th sampling instant. The output of the controller $v_{0(n)}$ after limiting to a safe permissible value is taken as amplitude of reference supply current A.

3.3 PWM Current Regulator

Current regulation loop is required for active wave shaping of input current to achieve unity input power factor and reduced harmonics.

3.4 Reference Supply Current Generation

The input voltage template B obtained from sensed supply voltage is multiplied with the amplitude of reference source current A in the multiplier-divider circuit. Moreover, a component of input voltage feed forward C is also added to improve the dynamic response of the converter system to line disturbances (fig. 2). The resulting signal forms the reference for input current. The instantaneous value of the reference current is given as:

$$i_s^* = AB/C^2 \quad (5)$$

3.5 Active Wave-shaping of Input Current

The inductor current error is the difference of reference supply current and inductor current ($i_{en} = i_s^* - i_s$). This error signal is amplified and compared to fixed frequency carrier wave to generate gating signals for power devices of the converter. PWM switching algorithm is selected depending on the converter topology.

4. MATHEMATICAL MODELING OF PFC BRIDGELESS BOOST CONVERTER

Two variants of bridgeless boost converter topologies are considered, ie, symmetrical and asymmetrical. Both types have identical characteristics. The variations lead to simplified current regulation in the symmetrical variant. The converter is described by two differential equations for inductor current i_L and dc link voltage across capacitor v_{dc} .

$$p\, i_L = (v_s - v_p - r\, i_L) / L \quad (6)$$

$$p\, v_{dc} = (i_p - v_{dc} / R)/C_d \quad (7)$$

where PWM voltage and current are as:

$$v_p = v_{dc} (S1 - S2) \quad (8)$$

$$i_p = i_L (S1 - S2) \quad (9)$$

respectively. Also S1 and S2 are switching states of switches S1 and S2, respectively.

5. ELECTROMAGNETIC INTERFERENCE FILTER

The Electro Magnetic Interference is transmitted in two forms: radiated and conducted. The switching converters supplied by the power lines generate conducted noise into the power lines that is usually several orders of magnitude higher than the radiated noise into free space. Metal cabinets used for housing power converters reduce the radiated component of the electromagnetic interference. Conducted noise consists of two categories commonly known as the differential mode and the common mode. The differential mode noise is a current or a voltage measured between the lines of the source, which is line to line voltage. The common mode noise is a voltage or a current measured between the power lines and ground that is line to ground voltage. An EMI filter is needed to reduce the differential mode and common mode noises. The filter comprises of inductors and capacitors as shown in Fig. 3(a).

6. SIMULATION RESULTS

The bridgeless boost converter system is simulated using Matlab Simulink. The AC source with EMI Filter is shown in fig 3(a). Noise is injected by using an additional source of higher frequency connected in series. Distorted input voltage is shown in fig. 3(b). The voltage waveform after EMI Filter is shown in fig. 3(c). The circuit diagram of open loop system with disturbance is shown in fig 4(a). Rotor speed curve is shown in fig 4(b). The circuit of closed loop system is shown in fig 5(a). Driving pulses for the MOSFET are shown in fig 5(b). Error signal is shown in fig 5(c). From the response of closed loop system, it can be seen that the speed reaches the set value.

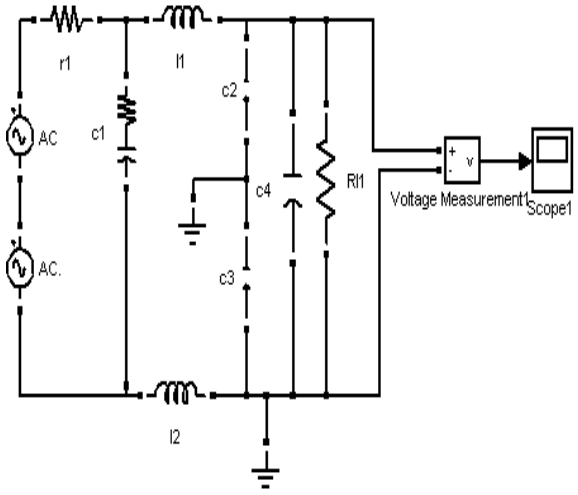

Fig -3(a): EMI filter circuit

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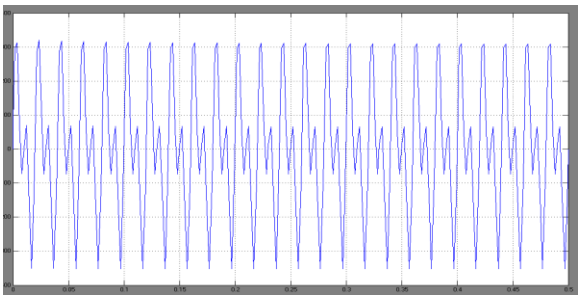

Fig -3(b): Input Voltage before EMI filter

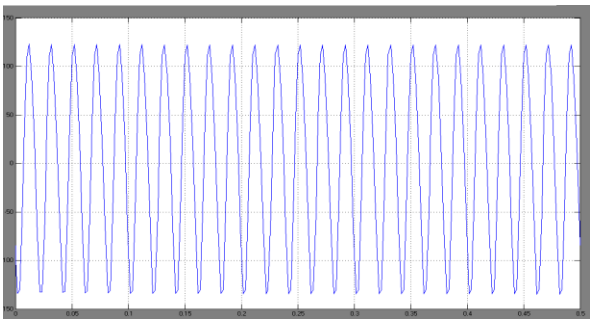

Fig -3(c): Voltage after EMI filter

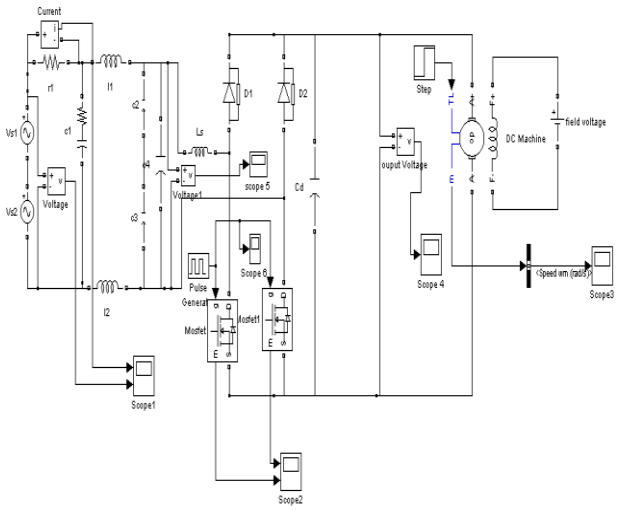

Fig -4(a): Simulation circuit of open loop system

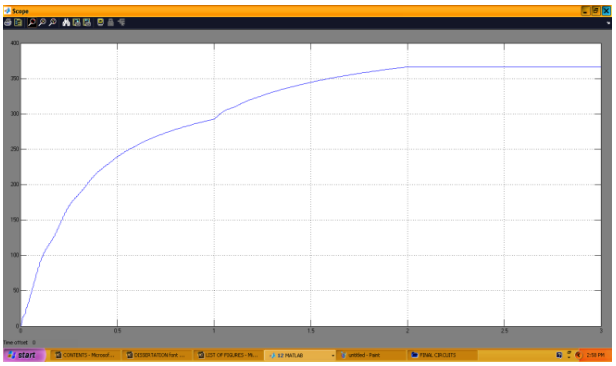

Fig -4(b): Rotor speed (Rad/Sec) with disturbance in open loop system

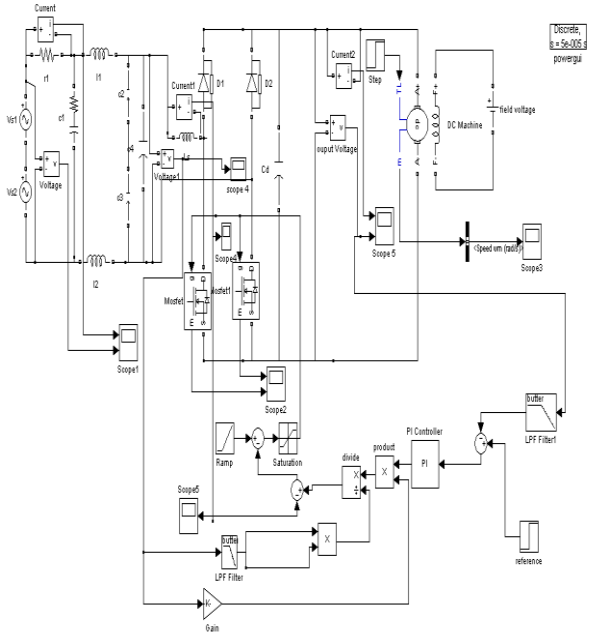

Fig -5(a): Circuit diagram for closed loop system

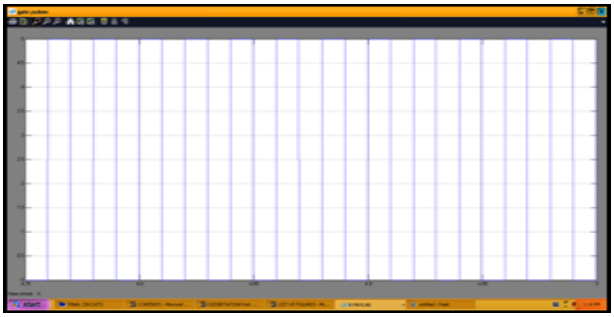

Fig -5(b): Output pulses

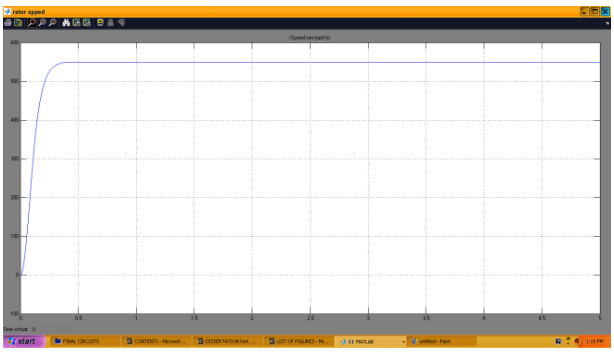

Fig -5(c): Rotor Speed (Rad/Sec) with Disturbance in Closed Loop System

7. CONCLUSION

The bridgeless boost converter fed DC drive is analyzed and simulated. The boost power factor correction (PFC) converter along with the Electro Magnetic Interference(EMI) Filter is also simulated. From the simulation results, it is observed that the best power factor can be obtained by using bridgeless

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boost PFC converter along with EMI Filter is a viable alternative for the control of DC motor. This circuit also has advantages like reduced hardware, high performance and improved power factor. The simulation results are in line with the predictions. This work has covered the simulation of open loop and closed loop controlled PFC converter. The hardware implementation will be done in future.

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