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A Review on Different Types of Multiplier Architecture

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***Abstract**: This paper presents a comparative analysis of three different multiplier architectures. The three multipliers architecture are array multiplier, a column bypass multiplier, and a array multiplier using Reversal Logic schemes. The multipliers are implemented on Spartan 6 FPGA. The architectures are compared in terms of critical path delay, power dissipation and area. The different multipliers are compared in terms of dynamic power consumption due to the scaling effects on leakage current. Each of the three multipliers has its own trade-offs between power and delay.*

***Keywords:** Low Power, Multiplier, Switching Delay, bypassing techniques, reversible logic*

1. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

It is well known that Multipliers consume maximum power in DSP computations [2]. Hence, it is very important factor for modern DSP systems to design low-power multipliers to reduce the power dissipation. In low-power multiplier design, many researcher experiments & find out results on the reduction of the switching activities [3] have been published. Besides that, a simple and straightforward approach [4] for low-power multiplier is to design a low-power Full Adder to reduce the power dissipation in an array multiplier. The other designs are proposed to reduce the power dissipation in a multiplication operation by interchanging dynamic operands [5] or using partially guarded computation [6]. Furthermore, the minimize of the power dissipation can also be achieved through the architectural modification via row bypassing [7] or column bypassing [8] techniques. Based on the concept of theory row and column bypassing techniques for the reduction of the power dissipation, a low-power 2- dimensional bypassing based multiplier [9] and a low-power row-and-column bypassing-based multiplier [10] are further proposed. However, the introduction of the extra bypassing circuits decreases the ability of minimize the power dissipation based on bypass extra bits to next steps.

2. RELATED WORK

The multiplication algorithm for an N bit multiplicand by N bit multiplier is shown below:

Y= Yn-1 Yn-2 .....Y2 Y1 Y0 Multiplicand
X= Xn-1 Xn-2 ..... X2 X1 X0 Multiplier
Generally:

Y= Yn-1 Yn-2 .....Y2 Y1 Y0
X= Xn-1 Xn-2 ..... X2 X1 X0
==========
Yn-1X0 Yn-2X0 Yn-3X0 ..... Y1X0 Y0X0
Yn-1X1 Yn-2X1 Yn-3X1 ..... Y1X1 Y0X1
Yn-1X2 Yn-2X2 Yn-3X2 ..... Y1X2 Y0X2
…… … … … …. …. …. …. …. ……..
Yn-1Xn-2 Yn-2X0 n-2 Yn-3X n-2..... Y1Xn-2 Y0Xn-2
Yn-1Xn-1 Yn-2X0n-1 Yn-3Xn-1..... Y1Xn-1 Y0Xn-1

AND gates are used to generate the Partial Products, PP, If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product. The way that the partial products are generated or summed up is the difference between the different architectures of various multipliers

Example:

```
    1101        4-bits

    1101        4-bits
-------------------------------
    1101
    0000
    1101
    1101
-------------------------------
10101001
```

For CMOS circuits, the power dissipation can be divided into static power dissipation and dynamic power dissipation. In general, static consumption is from the leakage current anddynamic consumption is from the switching transient current. For static power dissipation, the consumption is proportional to the number of the used transistors. For dynamic power dissipation, the consumption is obtained from the charging and discharging of load capacitance. The average dynamic dissipation of a CMOS gate is: $P_{avg} = ½ CfV_{dd}N$.

Where C is the load capacitance, f is the clock frequency, VDD is the power supply voltage and N is the number of switching activity in a clock cycle .Hence, it is very important for modern DSP systems to develop low-power multipliers to reduce the power dissipation In this paper we present a technique to minimize power dissipation in digital multipliers, concentrating on the switching activity. There have been proposed a lot of techniques to reduce the switching activity of a logic circuit.

A. Simple Array Multiplier:

Each partial product is generated by taking into account the Multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save

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algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits. Tabular form of 4x4 Array multiplier is shown in Fig. 1 4x4 Array multiplier.

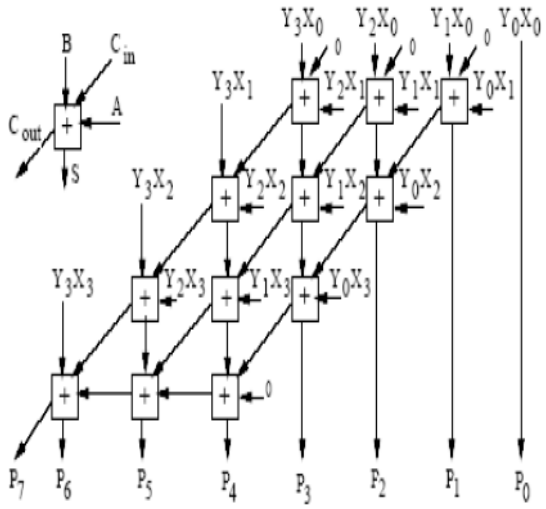

Figure 1: Array Multiplier

B. Column Bypass Multiplier:

We propose a multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0.

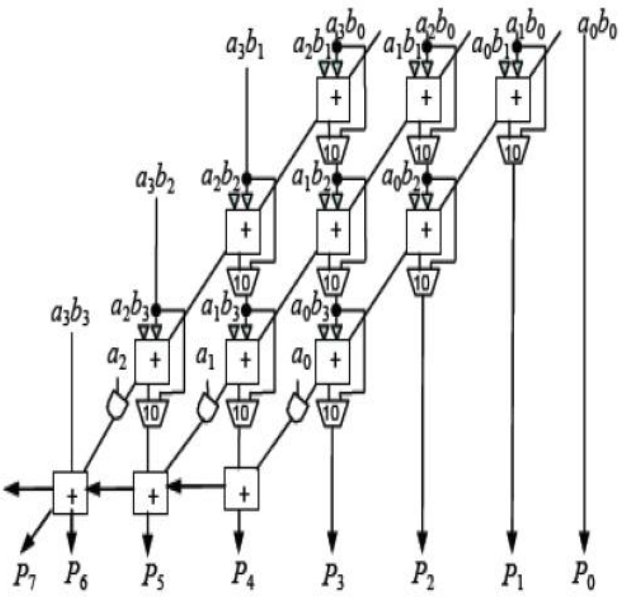

Fig 2: Column bypass multiplier

C. *Reversible Scheme Multiplier:*

Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design. They are also the fundamental requirement for the emerging field of the Quantum computing.

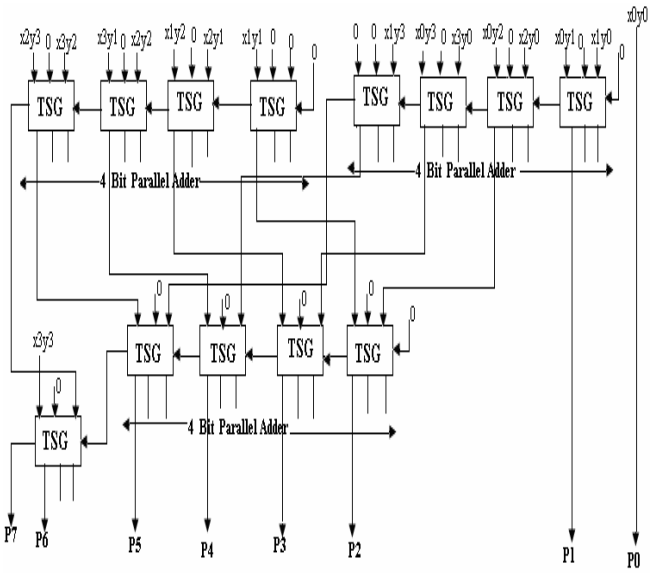

Figure 3: Reversible Multiplier

3. EXPERIMENTAL RESULTS

A. Analysis – Resource Utilization:

In all the multiplier designs, to give us an idea of the area that will be used, the number of transistors used in the circuit is counted since this directly affects the area. The results are shown in Table 1.

Table 1: Area overhead of different multiplier (4x4)

S.N.	Multiplier	No. of Slices Uses
1	Simple Multiplier	14
2	Bypass Column Multiplier	15
3	Reversible Gate Multiplier	16

B. Analysis - Power Dissipation

The average dynamic power of each test case were measured and tabulated in Table 2.

Table 2: Power dissipation in different multiplier (4x4) (mW)

S.N	Multiplier	Dynamic	Quiescent	Total
1	Simple Multiplier	9.14	13.76	22.90
2	Bypass Column Multiplier	7.86	13.76	21.62
3	Reversible Gate Multiplier	8.26	13.76	22.02

C. Analysis - Propagation Delay

For the propagation delay, the critical path delay is measured which occurs in the middle of the array. The test cases used travel along this path.

The propagation delay measured for each of the multiplier architecture is shown in Table 3.

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Table 3: Delay in different multiplier (4x4) (ns)

S.N.	Multiplier	Power Delay (nS)
1	Simple Multiplier	1.443
2	Bypass Column Multiplier	2.201
3	Reversible Gate Multiplier	3.359

4. CONCLUSION

Each multiplier has its own advantages and disadvantages. The multiplier with Simple braun has less delay compared to the array bypass multiplier, reversible but the Slices count is much higher and the added power from additional logic offsets the power saved. This also happens to the low-cost low-power bypassing based multiplier is performs better in both power and delay compared to Simple & reversible. The low power bypass multiplier performs best in terms of power reduction but worst at propagation delay among the tested multiplier is high. So above discussion in different multipliers in comparison in case of low power Bypass column multiplier better.

5. FUTURE WORK

In comparison of different Multipliers, Bypass multiplier is better but problem in power delay that can be realises in other multiplier such as row column bypass, 2 D dimensional multiplier & in used of high speed adder in place of simple full adders.

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