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Low Power and High Speed DCT/IDCT Using Radix 2 CORDIC Processor

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Abstract: *In Signal processing applications, DCT is the most widely used transform after DFT. The DCT/IDCT are important components in many picture compression and decompression standards, including H 263, MPEG, HDTV and JPEG. The application for these standards range from still pictures on internet to low quality videophones to high definition television. The DCT/IDCT also have applications in wide ranging areas as filtering, trans multiplexer, speech coding and pattern recognition. The major concern in DCT/1DCT architecture is method of implementing multipliers because of large number of multiplication operation, Which will consume more area and power. This paper describes a method of using Radix 2 CORDIC processor instead of multiplier which makes use of only shift and add operation. The proposed Architecture ie Radix 2 CORDIC implementation in DCT/IDCT, CORDCT(COR2DCT) Consumes less area and power and it is also of high speed compared to that of DCT/IDCT using multipliers. The proposed system is simulated and synthesized using Modelsim and also using CADENCE RTL complier tool. Analysis of area, delay ,and power has been done using CADENCE Tool. All these values have been compared with DCT/IDCT using multiplier it has been found that COR2DCT is area, power efficient and also of high speed.*

Keywords*: : Co-Ordinate Rotational Digital Computer(CORDIC), Discrete Cosine Transform (DCT), Joint Photographic Expert Group(JPEG) , PDP (Power Delay Product), EDP(Energy Delay Product), COR2DCT (Radix 2 cordic DCT).*

1. INTRODUCTION

DCT [1] has become one of the basic tools in signal and image processing, the popularity of which is mainly due to its good energy compaction properties. In particular DCT is the best substitute for Karhonen-loeve- Transform(KLT), which is considered to be statically optimal for energy concentration [2,3], where as Discrete Cosine Transform is optimal. The KLT is data dependent and requires more computation compared to the DCT. Due to this, Discrete Cosine Transform is finest substitute for KLT. The direct implementation of this is very expensive, which consumes more area and power. In row/ column approach multiplications have been reduced by decomposing into two sets of ID-DCT for an NXN block of data. The chen algorithm and similar algorithms, improve on the direct implementation of ID DCT/1DCT it makes use of 16 multiplication for an eight point ID DCT/1DCT. So an 8X8 row/column implementation requires just 256 multipliers for 2D DCT/1DCT. Matrix and vector approach makes use of 94 multiplication to compute 2D DCT. These are further reduced to 54 by computing scaled version of DCT. All these are difficult to implement in H/W. Some common power reduction tech which can be applied to are clock gating, pipeline and voltage scaling. There are different approaches which makes use of rotation based arithmetic, i.e CORDIC processor. As CORDIC uses only shift and add arithmetic VLSI implementation of such an algorithm is easily achievable. Implementing DCT using CORDIC algorithm reduces the number of computation during processing increases the accuracy of reconstruction of image and also reduces chip area of implementation of processor. This also reduces overall power consumption.

The remainder of this paper proceeds as follows Section 2 explains the Design Methodology of both CORDIC algorithm and DCT/IDCT algorithm. Details of the Architecture have been covered in Section 3. Section 4 covers the implementation of the Architecture , Simulation and Synthesis results. It has been concluded in Section 5.

2. DESIGN METHODOLOGY

2.1 CORDIC Algorithm

Co-Ordinate Rotational Digital Computer is abbreviated as CORDIC. The key concept is based on simple and ancient principles of two dimensional geometry. The interactive formulation of computational algorithm for its implementation was first described by J, Volder for the computation of trigonometric functions, multiplication and division.[7]

The basic CORDIC iterations used to determine cosine and sine functions are as follows.

$$X_{i+1} = X_i - d_i \sigma_i y_i 2^{-1}$$

$$Y_{i+1} = Y_{(i)} + \sigma_i X_i 2^{-i}$$

$$Z_{i+1} = Z_{(i)} - \sigma_i |\alpha_i| \quad (1)$$

Where $\alpha_i = \tan^{-2} 2^{-i} \sigma_i = (+1 \text{ or } -1)$

$$k = \prod_{i=0}^{n} \sqrt{1 + \sigma_i^2 2^{-2i}} \quad (2)$$

Above equations are used in rotating mode. In this vector is rotated by an angle θ to obtain new vector. In this mode, direction of each micro rotation is (σ_i) determined by Z_i. If sign of Z_i is positive then σ_i=1,, otherwise σ_i= -1 .

The parallel architecture which is used in DCT/1DCT is shown below in fig (1), as it is faster than sequential

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architecture and it also provides high throughput and low power consumption.[8,9]

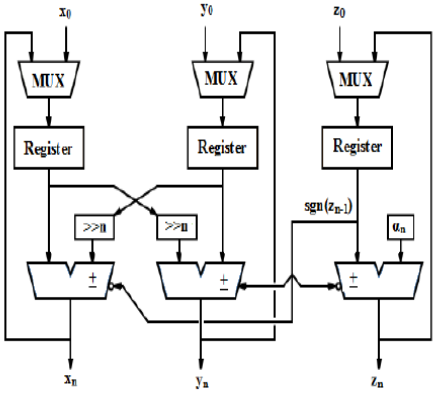

Figure 1: CORDIC hardware for one iteration

2.2 DCT/IDCT Algorithm :

DCT is very effective due to its symmetry and simplicity. Image is divided into blocks and each block is compressed using quantization. Equation (3) &(4) gives one dimensional DCT standard equations. One dimensional DCT:

The most common DCT definition of 1D sequence of length N is

$$c(u) = \alpha(u) \prod_{x=0}^{n-1} f(x)\cos\left[\frac{\pi(2x+1)u}{2N}\right] \quad (3)$$

u=0,1,2.....N-1.

Similarly inverse transformation is defined by

$$f(x) = \sum_{X=0}^{N-1} \alpha(u)c(u)\cos\left[\frac{\pi(2x+1)u}{2N}\right] \quad (4)$$

for x= 0,1,2....N-1.

α(u) = 1/√N for u=0

=√2/N for u =/0

from above equation u=0

c(0)= √1/N $\sum_{x=0}^{N-1} f(x)$

First transform co-efficient is the average value of sample sequence. This is termed as DC co-eff. All other transform co-efficient are called AC co-efficients. [4, 5]

Two dimensional DCT:

2D DCT is an extension of 1D and it is given by

$$c(u,v) = \alpha(u)\alpha(v) \sum_{x=0}^{N-1} \sum_{Y=0}^{N-1} f(x,y)\cos\left[\frac{\pi(2x+1)u}{2N}\right] Cos[\pi(2y+1)N/2N \quad (5)$$

$$f(x,y) = \sum_{u=0}^{N-1} \sum_{v=0}^{N-1} \alpha(u)\alpha(v)c(u,v)\cos\left[\frac{\pi(2x+1)u}{2N}\right] Cos[\frac{\pi(2y+1)V}{2N}] \quad (6)$$

3. ARCHITECTURES

A 2D DCT architecture and DCT architecture using Radix 2 CORDIC processor has been explained in this section

3.1 2D DCT: It is implemented using two ID DCT block and transposition block as shown in the fig (2) below. The 8x8 image matrix having the values in the range of 0-255 is first converted from unsigned to signed representations, which is called level shifting by subtracting from 128. The signed values are given as input to 1D DCT in either row or column wise. output of that is given to transposition block. then output of this is given to 2nd 1D DCT to obtain final output.

$Y = C \times C^T$ X - Input Matrix , C - Matrix Of DCT Co Efficient, C^{t} - Transpose Of C.

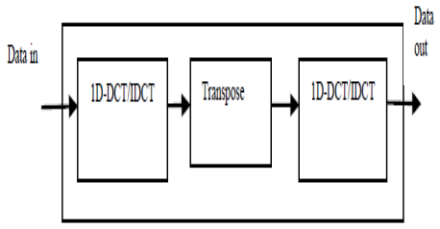

Figure 2: ARCHITECTURE OF 2D DCT

3.2 Radix 2 CORDIC DCT Architecture :

This section explains DCT architecture using Radix 2 CORDIC algorithm. The Radix 2 makes use of n iterations to calculate for n bit input. The latency to calculate cosine values is n cycles. Since the co- efficient of DCT are fixed. So it can be implemented using CORDIC. Totally 6 CORDIC processor are required.[6]

CORDIC (1) - π/ 4 CORDIC (3, 6) – 7π /16

CORDIC (2)– 3π/8 CORDIC(4, 5) – 3π /16

The following table gives detailed number of iterations and compensation in six CORDIC processors

Table 1: Algorithm Used for the Computation Of DCT

Processor	Angle	CORDIC iteration				
Cordic 1	π/ 4	-1,0				
Cordic 2	3π/8	1,0	1,2	1,3	1,6	1,7
Cordic 3,6	7π /16	1,0	1,1	1,3	1,10	
Cordic 4,5	3π /16	1,1	1,3	1,10	1,14	

TABLE 2: COMPENSATION ITERATIONS

	1	2	3	4	5
π/4	$1-1/2^2$	$1-1/2^4$	$1+1/2^8$	$1+1/2^9$	$1+1/2^{12}$
3π/8	$1/2^1+1/2^3+1/2^6$	$1/2^4$			
7π /16	$1/2^1+1/2^3$	$1/2^3+1$	$1+1/2^{12}$		
3π /16	$1-1/2^3$	$1+1/2^6$	$1+1/2^{10}$	$1+1/2^{12}$	

T The following figure (3) gives H/W implementation of CR2DCT.It makes use of 8 adders and 8 subtracters and 6 CORDIC processors.

4. IMPLEMENTATION

4.1 Mat lab Implementation:

The MATLAB has been used to read the image The original image is partitioned into block of small size 8 x8. As pixel value of image of image (black & white) range from 0-255. But DCT works on -128 to 127. This information is transformed form spatial domain to frequency domain using

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DCT. Quantization is achieved by dividing each element in the transformed image matrix by corresponding element in quantization matrix then rounding to the nearest integer value.

$C_{i,j}$; = round (Di; / $Q_{I,J}$, ;).

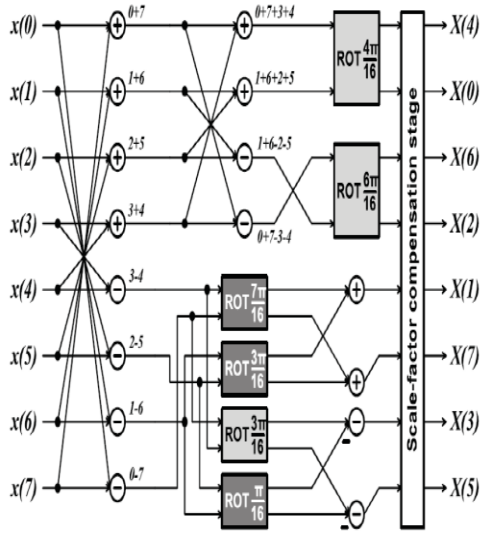

Figure 3: Hardware Architecture of COR2DCT

The co-efficient situated near the upper left corner corresponds to lower frequency to which the human eye is most sensitive of image block. Non- zero co-efficient will be used to reconstruct the image. The IDCT is next applied to matrix, finally 128 is added to each element of that result, resulting into original 8X8 image block. The comparison between output of IDCT and input image matrix shows that 70% of DCT coefficients were discarded prior to image block reconstruction.

4.2 Simulation Results:

Inputs to DCT core using CORDIC algorithm are generated using MATLAB is given from text file. The text file contain image dimension 512*512 pixels and size is 786 KB and output image has dimension i.e 512*512 pixels. Which is reduced to 47 KB without much degrading image quality. Both the DCT/IDCT blocks were written in Verilog and behavioral simulation has been observed using XILINX ISE Simulator. From PSNR table, it can be seen that using CORDIC in DCT / IDCT PSNR Value also is increased. PSNR value is 2 dB higher than that of using multiplier in DCT/1DCT.

Table 1: PSNR Values

PROCESSOR	PSNR(dB)
DCT/IDCT (MULTIPLIER)	40.2
DCT/IDCT(COR2DCT)	42.1

4.3 Synthesis Result (Xilinx) :

The Design is implemented on Xilinx Vertex 5 device. DCT operates at a speed of 169 MHZ with delay of 5.9 ns ,IDCT operates at 147.5 MHZ with delay of 6.8 ns, Whereas the DCT/IDCT Using multiplier operates at a speed 112 MHz and 129 MHz resp.

4.4 Synthesis Results (CADENCE):

CADENCE RTL Encounter is used to analyze Area, Speed and Delay. The following tables give comparison of DCT/IDCT using multiplier and using Radix 2 CORDIC processor (COR2DCT).

Table 2: Area, Delay and Power of DCT/IDCT using Multiplier

DCT Processor	Cell Area	Delay(ns)	Total power(mw)
DCT	25250	*7.86*	1.36710
IDCT	26271	*8.2*	1.38320

Table 3: Area, Delay and Power of DCT/IDCT Radix 2 CORDIC Processor

CRDCT Processors	Cell Area	Delay(ns)	Total power(mw)
COR2 DCT	12560	7.2	0.34685
COR2IDCT	13121	7.7	0.35434

Table 4: PDP, EDP and ADP of DCT/IDCT using Multiplier

DCT PROCESSOR	PDP	EDP	ADP
DCT	10.77	83.17	90432
IDCT	11.3	92.9	215422

Table 5: PDP, EDP and ADP of DCT/IDCT using Radix2 CORDIC Processor

CORDCT PROCESSORS	PDP	EDP	ADP
COR2DCT	2.5	17.9	90432
COR2IDCT	2.72	21.00	94471

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The performance of H/W architecture is evaluated with respect to Area, Delay and Power consumption. The Area, Delay and Power figure of Architecture are strongly interdependent. As a result, design constraints are often in conflict and tradeoffs have to be made. Tradeoff cost functions can be made between every combination of two or more measures to guide digital designers in accessing and selecting architecture that perform well in their system design space. The tradeoffs combinations are as follows PDP, EDP and ADP. PDP is average energy consumed per DCT transformation. A lower PDP means that power consumption is better translated into speed of each operation. and EDP represents that one can trade increased delay for lower energy of each operation. This also makes clear the strong coupling between delay and power which is the reason that many high speed techniques are useful for low power design.

5. CONCLUSION

The ASIC implementation of DCT/1DCT algorithm is carried out. It has been simulated and synthesized using Xilinx. and CADENCE RTL Compiler. Area, power and delay analysis has been done using RTL compiler with 90nm TSMC library. It can be observed that Radix 2 CRDCT processor uses 23% less hardware, then 41% reduction in critical path delay compared to that of DCT/IDCT using multiplier, and EDP shows that 88% energy saved. There is 53% decrease in ADP value also.

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