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Design of Asynchronous up-down, up-down Counter Using power efficient D-Flip Flop

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Abstract: *D flip flops are the basic memory element which is used in many of the applications. Due to increase in demand of portable devices the research in low power has tremendously increased. In this we have discussed about the existing 8T latch and proposed a new 9T flip flop with that latch which has reduced area and power when compared to the existing ones. With this proposed and existing flip flop an asynchronous up/down counter was designed. Power comparison was made between the counters where the asynchronous counter designed using proposed flip flop gives low power consumption when compared to the existing one.*

Keywords: *D flip flop, asynchronous counter, low power dissipation.*

1. INTRODUCTION

Latch is an electronic device which is used to store one bit of data information. When the clock pin at positive edge the output of the D flip-flop takes the state of the D input and delays it by one clock cycle. Hence it is known as delay flip-flop. Latches are used as buffers but flip flops are used as a registers. Flip flop is the basic memory cell which is used to store the value on the data line. It has an advantage that the output is being synchronized by a lock. Many logic synthesis tools use only D latch and D flip flop. As the use of D flip flop is very important in many devices and applications care should be taken to design it perfectly. The power consumption and area are the main criterion's considered while designing it. In today's world power dissipation became a major thing. In today's world power dissipation is the major problem as the high power dissipation leads to reduced time of operation, reduced mobility, high efforts of cooling, operational costs and reduced reliability. As the portable devices needs a good battery life time the low power consumption is needed. In digital systems counter circuits are used for many purposes. The number of occurrences of certain events is counted by using the counters and they generate timing intervals for control of various tasks in a system, keep track of time elapsed between specific events, Frequency synthesizers, frequency dividers and so on. Different types of counters are used in a variety of circuits. Here in this paper a 8 transistor D latch was discussed and from which a 9 transistor D flip flop is proposed and both the designs are compared and an asynchronous up/down counter was designed by using the existing and proposed D flip flop. Asynchronous counters are also called *ripple-counters* because of the way the clock pulse ripples it way through the flip-flops and they do not have a global clock like synchronous counter. The asynchronous up/down counter can change its state in either direction under the control of an select input i.e. up or down. The proposed and conventional designs are simulated and analysed in Hspice at 1 GHz (130 nm CMOS).

This paper is organised as follows: Section II reviews the latch design. Section III describes about the asynchronous counters. Section IV summarizes the results and comparisons. Section V concludes the paper.

2. LATCH DESIGN

The 8 transistor static latch uses the pass transistor logic instead of transmission gate, and thus two transistors are less. In this design, the transistor PMOS_1 at the input side takes the data input and passes when the clock signal is low. The NMOS_1 is forming the feedback loop. The transistor NMOS_3 is passing the signal when clock signal is high and transistor PMOS_3 is passing the intermediate signal when clock signal is low. NMOS transistors are weak 1 and PMOS transistors are weak 0. Thus pass transistor logic gives threshold loss problem but this can be overcome by the inverters in the circuit. Output QB. Suffers with some threshold loss problem and that is verified during simulation, but output inverter compensates this problem and output waveform of Q is not showing any threshold loss. The proposed 8T latch is negative level triggered.

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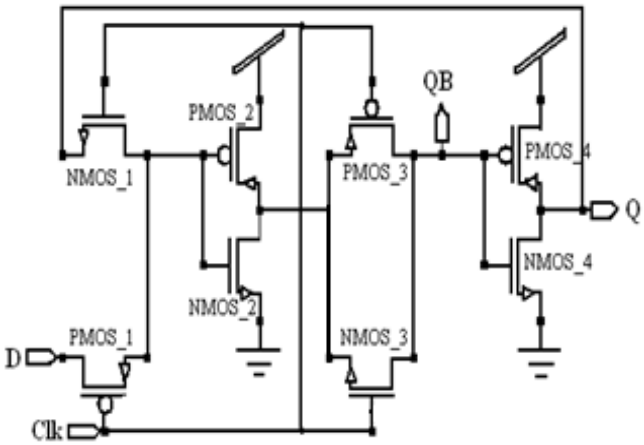

Figure1: 8-TransistorLatch Design.

The master slave flip flop consists of two stages and it is given as:

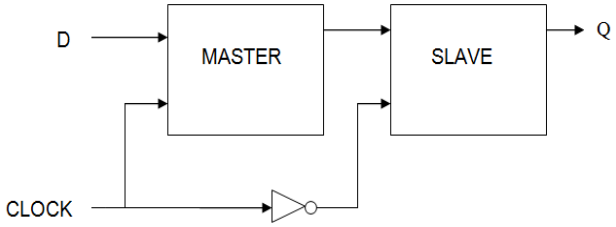

Figure 2: Master Slave flip flop.

The first stage of the flip flop is the master which is driven by the clock signal, while the second stage is the slave which is driven by the inverted clock signal. Thus the master stage is positive level sensitive and the slave stage is negative level sensitive. When the clock signal is high, the master stage follows the D input while the slave stage holds the previous value. When the clock signal changes from logic '1' to logic '0', the master latch samples the D input and stores the value at the time of the clock transition. At this time the slave latch becomes transparent, passing the stored master value to the output of the slave stage. at this stage the input is not affected by the output because the master stage is disconnected from the input D. when the clock signal changes from logic '0' to logic '1', the slave latch takes the master latch output and the master latch starts sample the D input again.
The flip flop using this latch consumes more area and power as it contains both the master and slave unit and it is given as:

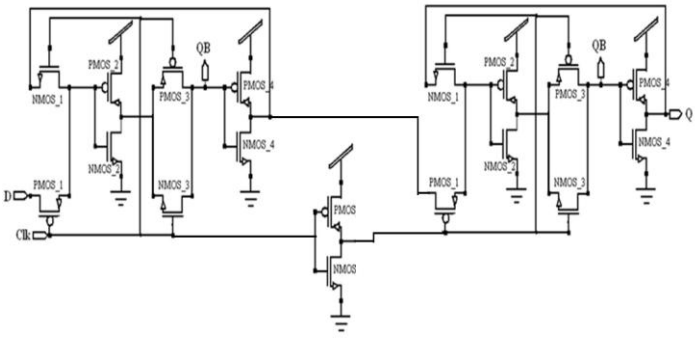

Figure 3: Flip flop using 8-Transistor latch.

The proposed 9 transistor flip flop is a master slave flip flop which has to be used in counters. It consists of two stages i.e. master and slave.

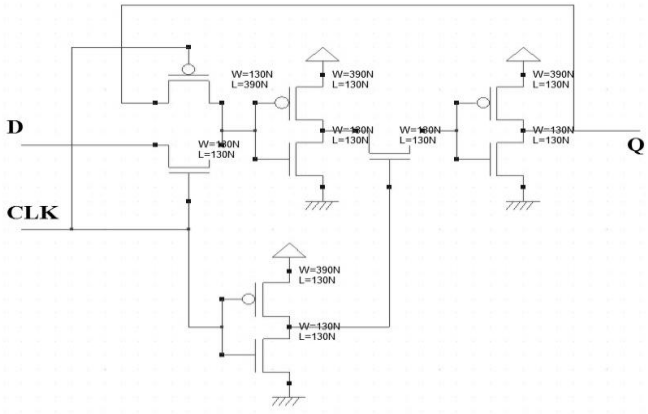

Figure 4: Proposed 9 transistors flip flop.

When the clock is at logic 1 the master will function and produces the output. Then when clock is at logic 0 the slave will take the output of master as input and produces the output. This flip flop when compared to the existing one consumes less area and power.

3. COUNTER DESIGN

A counter is a circuit that produces a set of unique output combinations corresponding to the number of applied input pulses. The number of unique outputs of a counter is known as its mod number or modulus. Generally D flip flops or Toggle flip flops are used to design the asynchronous counters. They are called "Asynchronous Counters" because the clock inputs of the flip-flops are not driven by the same clock signal. Asynchronous counters are sometimes called ripple counters because the data appears to "ripple" from the output of one flip-flop to the input of the next. A fundamental performance advantage for asynchronous circuits is that the variability in delays associated with these computation steps. A synchronous circuit is either quiescent (i.e., the clock is turned

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off) or active entirely (i.e., clock on). An asynchronous circuit, in contrast, only consumes energy when and where active. Any sub circuit is quiescent until activated. After completion of its task, it returns to a quiescent, almost non dissipating state until a next activation. The term Asynchronous refers to events that do not occur at the same time. According to counter operation, asynchronous counters means that the flip-flops within the counter are not connected in a way to cause all flip flops states at exactly the same time, they are wired in such a way that links the clock of the next flip flop to the Q of the present device. This causes the output count states to ripple through the counter. An up down counter uses a multiplexer in between the flip flops for the up and down counting control signal. The multiplexer used here is of a low power transmission gate multiplexer.

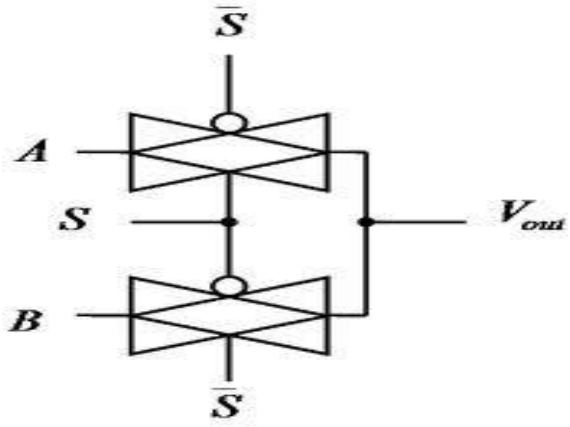

Figure 5: Transmission gate multiplexer.

The asynchronous counters using the existing flip flop is given below which has the area and power overload. The multiplexer connected between the flip flops in the up/down counter to provide the up down counting. When the selection signal is at logic 1 the counter works as an up counter and when it is at logic 0 it operates as down counter.

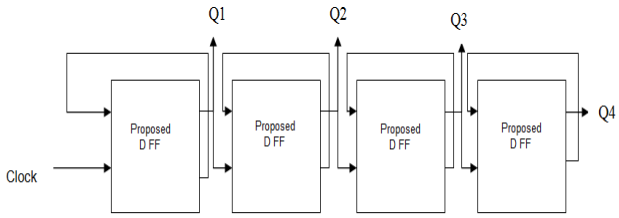

Figure 5: Up counter using proposed D flip-flop.

The up counter counts from 0000 to 1111. Here the input to each stage is its Q bar output and clock is given only to the first stage. The clock to the remaining stage is the Q output of the previous stage. This consumes less area and power when compared to the counter designed using the existing D flip flop. The asynchronous down counter using the proposed D flip flop is given below which counts from 1111 to 0000. The clock signal to first stage is given directly and to the following stages the Q bar output of the previous stage is taken and it is given as the clock signal.

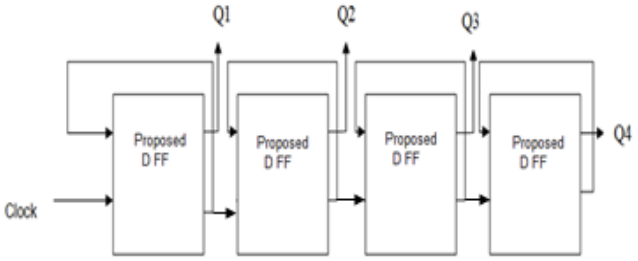

Figure 7: Down counter using the proposed D flip flop.

The asynchronous up/down counter is given below. This counts from 0000 to 1111 and 1111 to 0000 depending on the selection line. This selection line is given to the multiplexer as selection line and the Q and Q bar outputs of the flip flops are given as inputs to the multiplexer. Depending on the selection line the multiplexer selects the Q or Q bar output and gives as the clock signal to the next stage.

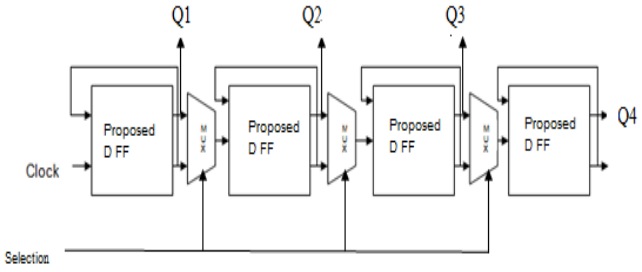

Figure 8: Up/Down counter using proposed D flip flop.

The proposed counter is less in area and power when compared to the existing one because the existing using the 8 transistor latch in both master and slave mode so the area increases i.e. 18 transistors for each flip flop but the proposed flip flop is a master slave which uses only 9 transistors.

4. RESULTS AND COMPARISION

The simulation is done by HSPICE and the output waveform for the existing counter and proposed counter is given below.

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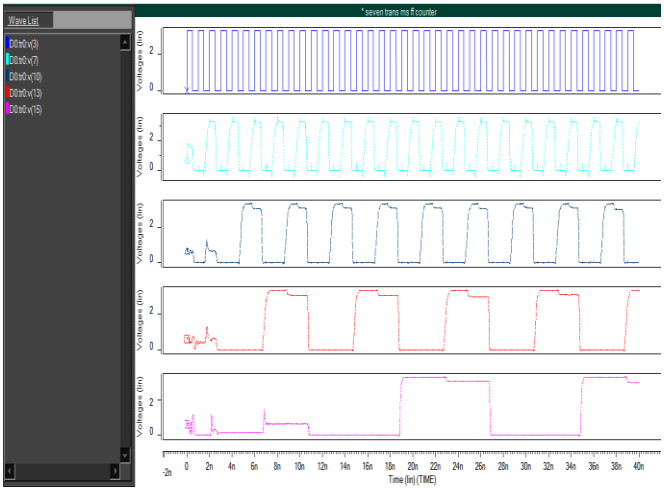

Figure 9: Output waveform of proposed down counter.

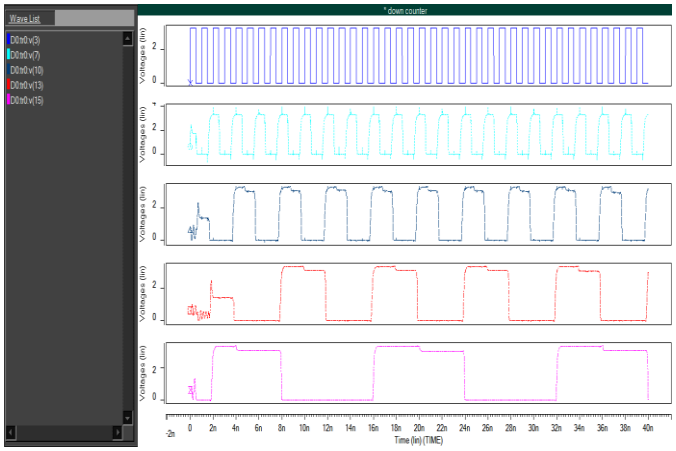

Figure 10: Output waveform of the proposed down counter.

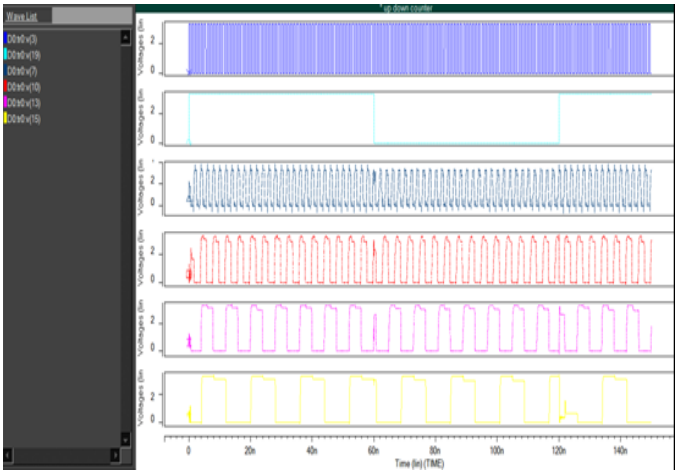

Figure 11: Output waveform of proposed up/down counter.

The power comparison is made between these flip flops and counters. While the proposed model gives the low power and less area.

Table 1: Power and transistor comparisons of flip flops.

FLIP-FLOP	TRANSISTOR COUNT	POWER CONSUMPTION
Existing D flip-flop	18	9.536e-05
Proposed D flip-flop	9	4.054e-05

Table 2: Power comparison of the counters.

COUNTERS	USING EXISTING D FLIP-FLOP	USING PROPOSED D FLIP-FLOP
Up counter	2.295e-04	1.641e-04
Down counter	2.329e-04	1.338e-04
Up/down counter	2.501e-04	1.533e-04

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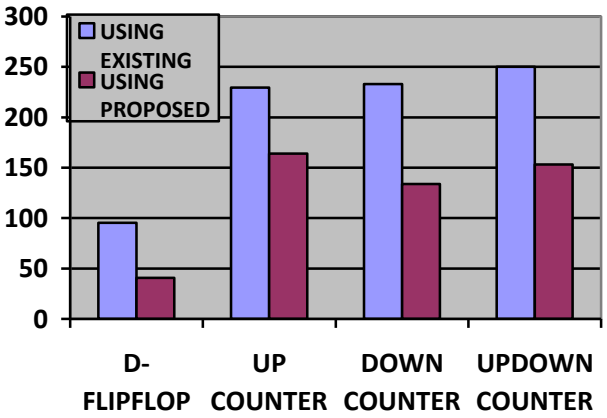

Figure 12: Power comparison graph of counters.

5. CONCLUSION

In this paper we have designed the 9-Transistor DFF using which the up, down, up/down counter has been designed and simulated in 130nm CMOS technology with HSPICE tool. From the comparison table it is clear that the proposed design has less power consumption in terms of power.

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