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Energy Recycling for Large Chip Design Using Low Power Switching Converters

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Abstract: *This project aim is to develop a low-skew in multigiga hertz clocks circuit operating with large digital chips. A capacitance can be charged from the supply and then discharged to ground. In large digital chips amount of wastage in capacitor is high due to number of connections. Hence we can use an energy recycling concept to reduce the overall power consumption. By this energy recycling the wastage energy is used by the other part of the chip. For this energy recycling integrated clock driver and converter network are merged. With using of multigiga hertz the reduced size obtained in the inductor and capacitor without loss and 42% of energy saving will occur. This concept is implemented by the 180nm cadence tool.*

Keywords: *Energy Recycling, Multigiga hertz clock, Clock Driver and Buck Converter*

1. INTRODUCTION

The energy consumption in large chips are keep on increasing and need of the large chips with thin gate oxides are take an essential part in the design and applications. It can lead to increasing in the frequency usage. In the integrated clock and buffer concept [1] is well and reducing the power. But in large chips it will increasing the chip area because we have to done multiple number of integrated clock driver and buffer network.
So we are in the need of solution to this problem. To address and clear this difficult in large chips our driver/converter circuit with energy recovery concept are very well use. To reduce the clock energy in circuits lot of inventions keep on going some of are, double edge triggered flip-flops, low-swing signaling ,clock gating, adiabatic switching [2], and resonant clocking [3], [4]. Compare to the above methods our concept can reduce the overall energy. For recover and redeploying this capacitive stored energy, we develop a merged buck converter circuit and clock driver. One of the main advantage is on chip recover voltage is differ from the power supply with low.

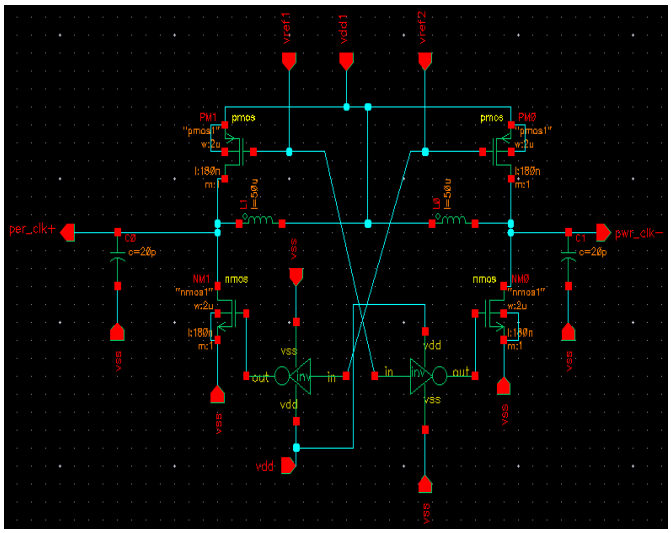

Figure1: Existing Method Clock Driver Schematic

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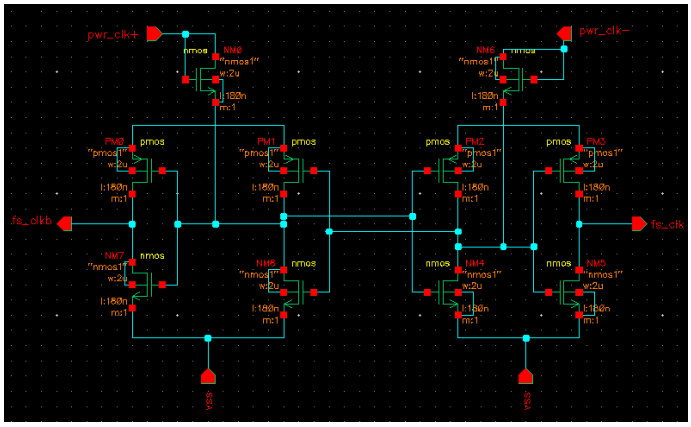

Figure2: Existing Method Clock Buffer Schematic

Right below the title from the fig 1 and 2 we can easily know the practical chip area, power and delay increasing while they implement in large chips. Our project is made compatibility and lap between dc-dc converter and switching converters.

To step up our goal switching frequencies have been increasing steadily to shrink the size of the required passive output filters. In this approach clock node is directly use since justification of high frequency, high capacitance and power overhead is occurred.

The clock driver and a converter are similar but both act as a tapered chain inverter to drive large final inverter. The important difference is that clocks normally maintain a fixed duty cycle, while duty cycle to output voltage varies by the converter. To produce a dc output waveform with low ripple converter attach a large LC output filter but clock output is a high quality square waveform.

Normally large chips/circuits are using a multiple clock buffer and driver circuits, Instead of using a large network of it. Hence our approach is do a good thing in in multiple clock buffer and driver circuits. It can reduce the overall power consumption and need of multiple clock circuits. Gating is one of the clock concepts but it requires local clock that is called as gaters. Our converter covers roughly 1mm*mm of area with local gated regions.

2. SIMPLIFIED CIRCUIT

Simplified version of merged clock driver and clock shown in fig 3. A delay element is introduced to provide ZVS during the high to low transition due to large amount of capacitance Cclk. If source drain voltage reaches 0v, ZVS saves energy if Mn is turned on. The operation of buck converter by average pulse width modulated voltage through a low passive filter. The capacitance of a clock node and stray capacitance of Mn and Mp include in the overall capacitance Cclk.

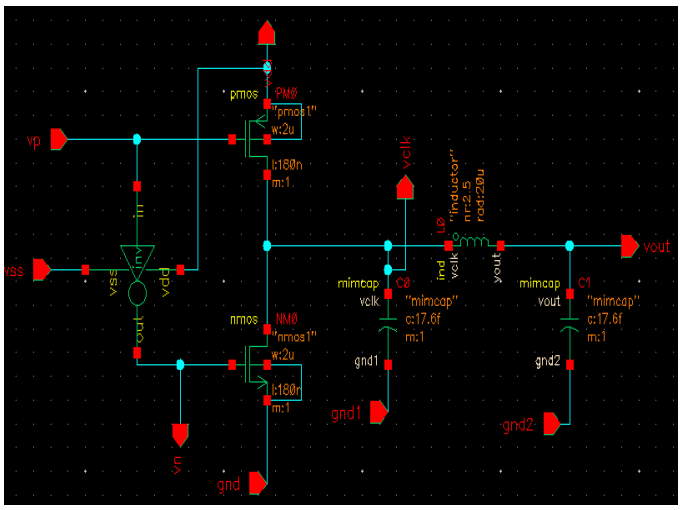

Figure 3: Proposed Clock Driver/Converter Schematic

The idealized timing diagrams shown yhe operation of the circuit. Clock duty D, switching period T_{sw} , and ZVS delay time T_{delay} are calculated by cadence output waveforms.

3. OPERATION

1) Phase -1

Time limit- 0 to $D\times T_{sw}$ the load is drive via Lf and Cf, charged through Cclk Mp. The voltage across the inductor is constants while current incrersres in it.

2) Phase -2

Tile limit- $D\times T_{sw}$ to $D\times T_{sw}+T_{delay}$ this is for energy recycling, Mn and Mp both are off during this time, Lf as the inductor current cannot disrupted abruptly by this rapid drop of Vclk is achived. Cclk would be discharged to ground at time $D\times T_{sw}$ through mn if no delay is present.

3) Phase -3

Time limit- t$D\times T_{sw}+T_{delay}$ to T_{sw} this phase will act when voltage across Mn is close to zero. But Mn provides virtual ground at node Vclk while conducting in reverse. While source drain voltage often close to zero, Zvs operation occurred when Mn is turned on, thereby reducing dynamic power loss. Mp is turned on –ve inductor current charging in C clk. No ZVS operation is implemented for Mp. The converter always operates in conduction mode.

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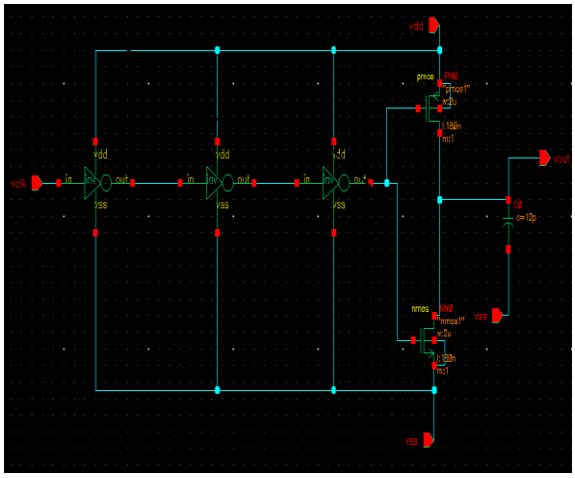

Figure 4: Reference Clock Driver

Merging the clock transistor has the same transistor and Cclk load as the merged design $V_{out} = D \times V_{D\ D.}$ In both circuits NMOS transistor lesser than PMOS transistor, except for the last inverter stage in which the PMOS in 4 times wider to reduce voltage drop across Mp while Vclk is high and current is building up in the inductor Lf.. NMOS transistor gate capacitance is used to implement the converter filter capacitor Cf while the gate capacitance of a simple large, inverter is used to response the parasitic and load capacitance at the clock node Cclk.

3.1 Timing Diagrams:

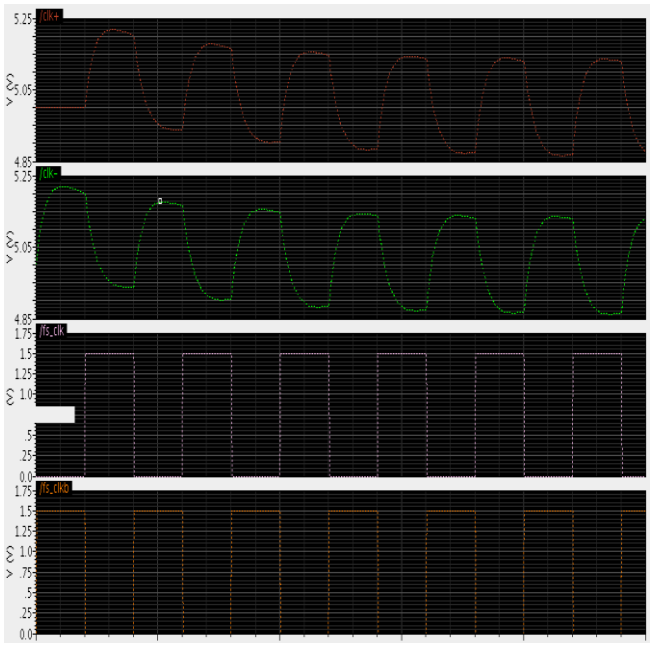

Figure 6: Existing Timing Diagram

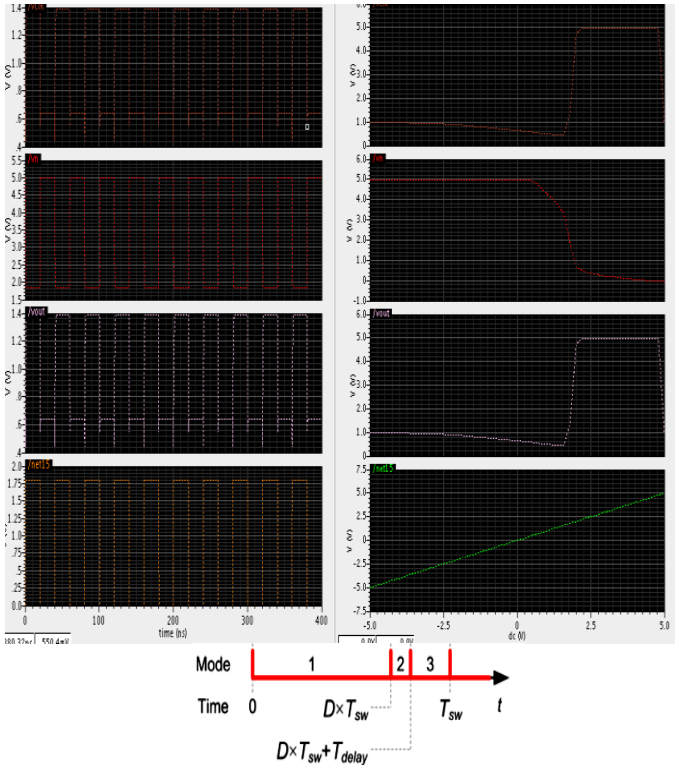

Figure 5: Proposed Timing Diagram

In the existing method in order to satisfy high current requirements, several LC drivers should be drive differential blocks to perform correctly. This will increase the area overhead associated with the inductors. We can implement inductors on top to reduce the area overhead but it will lead to reduction in quality factor. From this idealized diagrams we can easily calculate the timing values. The comparison between the proposed and existing scheme shows that reduction in overall power, chip area and clock period minimization are achieved.

4. CONCLUSION

Merging the functionality of the switching dc–dc converter with the clock driver energy recovery from a clock load has been shown to be possible. Integrated clock driver/converter circuit recycling the clock energy by employing the clock capacitance as a ZVS capacitor for the main inverter. The output filter taking only a small area of chip estimated to be 15% of the functional island area, such merged clock and dc–dc converters. The clock driver and converter to share the tapered driver chain, significant energy is achieved. Retaining the fast switching edges necessary for a high-quality square wave clock waveform because the tapered drier used here gives sufficient drive to the main MOSFETs.

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