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LOW POWER PULSED HYBRID FLIP-FLOP DESIGN USING GDI TECHNIQUES

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Abstract: *In this paper, we introduce a new Pulsed Hybrid Flip-Flop (PHFF) using Gate-Diffusion-input (GDI) technique. This allows to reducing power-delay products and area of the new PHFF circuit, while maintaining the low complexity of logic design. The proposed design eliminates the large capacitance present in the pre-charge node. The performance comparisons made in 180nm technologies using Cadence tool. The proposed PHFF offers a power reduction of 26% and 32% reduction in power-delay product in GDI. PHFF are compared with other flip-flop designs by implementing a 4-bit Ring counter and 4-bit Johnson up-down counter.*

Keywords: *Gate-diffusion-Input technique, Power-Delay product, Flip-Flop, Complexity*

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1. INTRODUCTION

A. Gate-Diffusion-Input Techniques.

Technology and speed and performance of the system are always moving forward, from low scale integration to very large scale integration and from few megahertz to gigahertz. In VLSI technology, we can consider the three factors. These are area, Delay, speed/performance and power requirement. Now a day's various techniques are used to attain these factors in VLSI technology. In this proposed PHFF area and power dissipation are reduce by using GDI techniques.

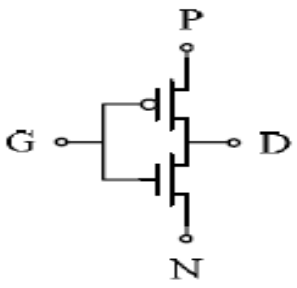

Figure 1: GDI basic cell

Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high-performance and low-area implementations of basic memory components. In both analog and digital circuit, flip-flop is used to store the data. D-Flip-Flop is most commonly used in various applications. Various DFF circuits were researched and presented in the literature [1][3][4], aiming to achieve an optimal design in terms of delay, power and area. Some efficient techniques were developed and adopted by designers for a variety of technologies [1]. Gate-Diffusion-Input(GDI) design technique that was recently developed and presented in [2], proposes an efficient alternative for logic design in standard CMOS and SOI technologies.

The GDI method is based on the simple cell shown in fig 1. A basic GDI cell consist of four terminals- G (It is common input of the both nMOS and pMOS transistor's gate terminals), N (the outer Diffusion node of the nMOS transistor), P (the outer diffusion node of the pMOS transistor) and the D node (the common diffusion of both type of transistor).

N	P	G	D	Function
'0'	B	A	$\overline{A}$B	F1
B	'1'	A	$\overline{A}$+B	F2
'1'	B	A	A+B	OR

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B	'0'	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table 1: some logic functions that can be implemented with a single GDI cell.

Table 1 shows how various configuration changes of the inputs P, N and G in the basic GDI cell correspond to different Boolean functions at the output D. GDI enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and PTL design techniques [2]. Multiple-input gates can be implemented by combining several GDI cells. The buffering constraints, due to possible V_{TH} drop, are described in detail in [2], as well as technological compatibility with CMOS and SOI.

B. Analysis of Flip-Flop architectures.

A large number of flip-flops have been designed and implemented in past few decades. They can be grouped under the static and dynamic styles. Most of the flip-flop are designed in Master-Slave connections, such as the transmission gate based master-slave flip-flop in [6] and PowerPC master-slave latch in [7]. They are dissipating comparatively lower power and have a low clock-to-output (CLK-Q) delay. Extensive work has been devoted to improve the performance of the flip-flops in the past few decades [1],[3]-[8].

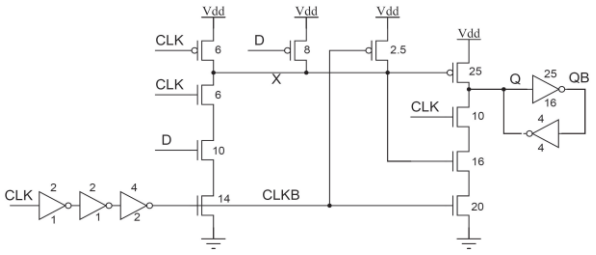


Figure 2: HLFF

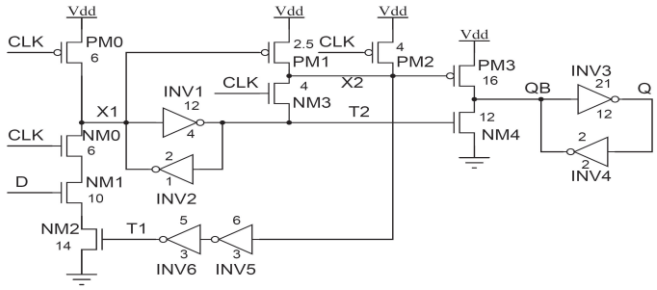


Figure 3: CDMFF

In a synchronous system, the delay overhead associated with the latching elements is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here D-Q delay refers to the sum of CLK-Q delay and setup-time of the flip-flop. Hybrid latch flip-flop (HLFF) [1] and conditional data mapping flip-flop (CDMFF) [2] are shown in fig2 and fig3, they are considered as the classic high-performance flip-flops. Several hybrid flip-flop designs have been proposed in the past decade, all aiming at reduction of power, delay, and area.

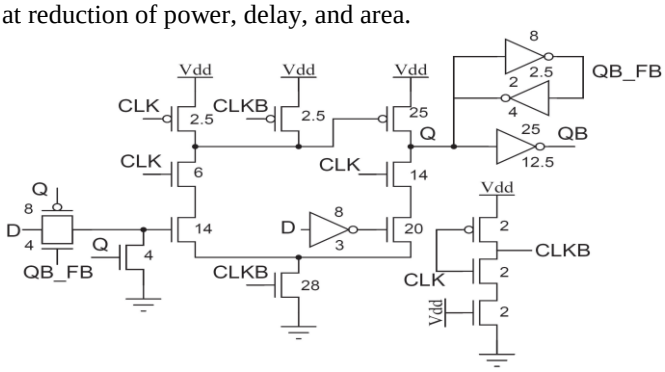
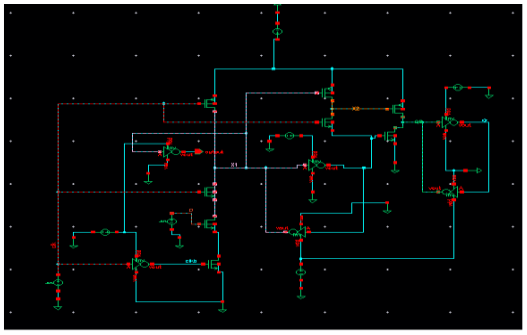


Figure 4: XCFF

A recent paper [4] introduced a flip-flop architecture named cross charge control flip flop (XCFF) shown in fig4, which has considerable advantages over HLFF in both power and speed. It uses a split-dynamic node to reduce the precharge capacitance, which is one of the most important reasons for the large power consumption in most of the conventional designs. But this structure still has some drawbacks, due to redundant power dissipation that results when the data does not switch for more than one clock (CLK) cycles. Also, the large hold-time requirement makes the design of timing-critical systems with XCFF an involved process. Duel dynamic node pulsed hybrid flip-flop (DDFF) is shown in fig 5. It eliminates the drawbacks of XCFF. This flip-flop is free from unwanted transitions resulting when the data input is stable at zero. DDFF requires high power consumptions and overall chip area.



. Figure 5: DDFF

The first category of the flip-flop are designed in static style and second category of the flip-flop design, the dynamic flip-flops include the modern high performance flip-flop [1]-[3]. This flip-flop is purely dynamic designs as well as pseudo-dynamic structures. The latter, which has an internal precharge structure and a static output, deserves special

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attention because of their distinctive performance improvements. They are called the hybrid structures, because they consist of a dynamic frontend and a static output. The benefit from the CLK overlaps to perform the latching operation.

The major source of power dissipation in the semi-dynamic designs are the redundant data transitions and large precharge capacitance, CDMFF comes under this section. The large precharge capacitance in a varies type of designs result from both pull-up and pull-down transistor are driven by precharge node. The common drawback of many conventional designs was considered in the design of XCFF. It reduces the power dissipations by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors.

In this paper a new implementation of PHFF using GDI technique is presented. This new PHFF design allows reducing power-delay product and area of the circuit, while maintaining low complexity of logic design. GDI PHFF is compared with other design techniques with respect to gate area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI implementation. The circuits have been implemented in 180nm technologies and simulated to compare the proposed GDI structure with existing by using cadence tool.

This paper can be divided as fallows. Section II describes the proposed PHFF architecture based on GDI technique and its operation was provided. Section III describes the performance analysis. Section IV descries the simulation result and comparison table. Finally conclusions and future work are discussed in section V.

2. GDI TECHNIQUE BASED PHFF IMPLEMENTATION AND OPTIMIZATION

A novel implementation of a GDI technique based PHFF is shown in fig6. It based on the master-slave connection on two GDI latches. Each cell consists of four basic GDI cells, resulting in a simple eight-transistor structure.

The components of the circuit can be divided into two main categories. These are body gates and inverters. Body gate are responsible for the state of the circuit.

These gates are controlled by the CLK signal and create two alternative paths: one for transparent state of the latch (when the CLK is low and the signals are propagating through PMOS transistors), and another for the holding state of the latch (when the CLK is high and internal values are maintained due to conduction of the NMOS transistors).

Inverters are responsible for maintaining the complementary values of the internal signals and the circuit outputs. An additional important role of inverters is buffering of the internal signals for swing restoration and improved driving abilities of the outputs.

This partition to categories can be helpful for understanding of circuit operation and optimization. A scan be seen, in body gates the transmission of the signal is performed through the diffusion nodes of the GDI cells. It might cause a swing drop of V_{TH} in the output signals. This problem is solved by the internal inverters in their buffer role. Performance optimization of the proposed circuit can be performed by adjusting the transistor sizes (as sweep Parameter in simulation) to obtain a minimal power delay Product. This procedure is iterative and contains a sequence of separate size adjustments: First, the same scaling factor is obtained for all transistors of the circuit (body gates and inverters).Secondly, iterative size optimizations are applied separately to inverters and body gates (mostly by opposite shifting of the scaling factors around the "operation point" found in first adjustment), while targeting the minimal power-delay product. For high load requirements, an additional optimization can be separately performed on the inverter of the Slave latch. The relatively compact structure of the proposed PHFF, containing 18 transistors (with the inverter for complementary value of D), makes it an efficient alternative for obtaining the combination of low area and high performance

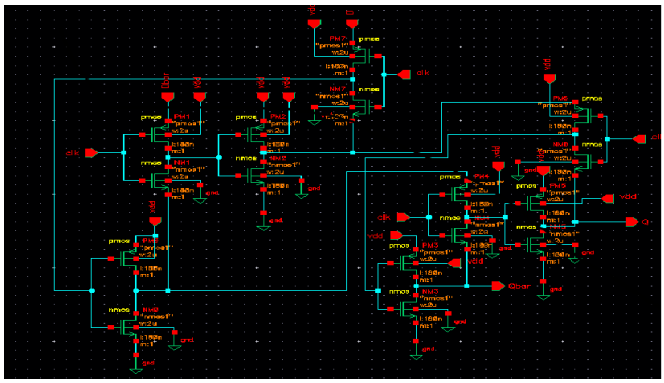

Figure 6: Proposed PHFF

The operation of proposed PHFF can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when clock is high. The actual latching occurs during the 1–1 overlap of D and $\overline{D}$ during the evaluation phase. If D is high prior to this overlap period, node $X1$ is discharged through NM0,4. This switches the state of the cross coupled inverter pair INV1-2 causing node $X1$to go high and output $\overline{Q}$to discharge through $NM2$. The low level at the node $X1$ is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node $X2$ is held high throughout the evaluation period by the pMOS transistor $PM1$. As the CLK falls low, the circuit enters the precharge phase and node $X1$ is pulled high through $PM0$, switching the state of INV1-2. During this period node $X2$ is not actively driven by any transistor, it stores the charge dynamically. The outputs at node $\overline{Q}$and maintain their voltage levels through INV3-4.

If D is zero prior to the overlap period, node $X1$ remains high and node $X2$ is pulled low through $NM3$ as the CLK goes high. Thus, node QB is charged high through $PM2$ and $NM4$ is held off. At the end of the evaluation phase, as the CLK

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falls low, node $X1$ remains high and $X2$ stores the charge dynamically.

The setup time and hold time of a flip-flop refers to the minimum time period before and after the CLK edge, respectively where the data should be stable so that proper sampling is possible. Here setup time and the hold time depend on the CLK overlap period. If VM is the switching threshold of the inverter pair INV1-2 and T_{vm} is the time required to discharge node $X1$ to VM, the hold time required by the flip-flop can be expressed as

$$T_{hold1} \geq T_{vm} \quad (1)$$

$$T_{hold0} \geq T_{ov} - T_{vm} \quad (2)$$

Where T_{ov} is the overlap period defined by the low to high transition of the CLK and high to low transition of CLKB. It should be greater than T_{vm} for the proper functioning of the flip-flop T_{hold1} and T_{hold0} represent the hold-time required for sampling a one and a zero, respectively. Also note that T_{hold1} and T_{hold0}, respectively are the maximum time period after the CLK transition such that the flip-flop samples a zero and a one, respectively. Now the overlap period can be chosen such that T_{hold1} and T_{hold0} in (1) and (2), respectively.

3. PERFORMANCE ANALYSIS

To analyze the performance of PHFF, other designs were also simulated under similar conditions. Since the D-Q delay reflects the actual portion of the time period consumed by the latching device. Optimum setup-time is the data-to-CLK delay when D-Q is at its minimum. As mentioned by Stojanovic and Oklobdzija [7], the power is divided into three parts–the latching power, the local CLK driving power, and the local data driving power, to accurately analyze the power-performance of various designs. The simulations are carried out at various data activities to obtain a realistic performance comparison of various designs.

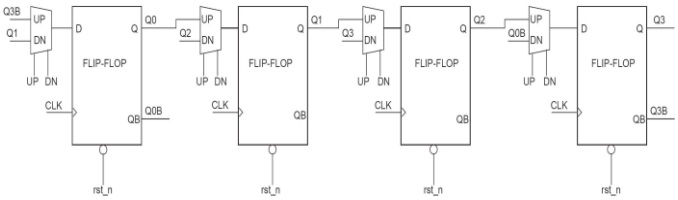

Figure 7: 4-b synchronous up-counter

A data activity of 100% represents an output data transition at every positive CLK edge, and 0% represents no data transition. Since the performance of the proposed flip-flops depends on the CLK overlap period, a detailed analysis at various process and temperature corners is carried out. Also, the process variation impact on the power and latency of the flip-flop is studied in detail from a 1000-point Monte-Carlo simulation with mismatch between transistors. Here, power and D-Q delay were measured when the flip-flop was working at optimum setup-time. Results with and without a setup time margin are provided to understand the importance of system design with process variations in mind. Since static leakage power is one of the main sources of power dissipation at scaled down technology nodes, comparison of the leakage performance of various designs has been carried out.

The leakage currents for different input and output conditions are measured to find the worst case leakage power. In addition, all the designs were analyzed at different voltage points to understand the impact of supply voltage fluctuation in the functionality of the flip-flops. Finally, a 4-b synchronous up-counter is designed to highlight the performance of the proposed flip-flop architecture. The reason for considering a counter is that the data activity at each bit position is known. The most significant bit has the least data activity (12.5%), whereas the least significant bit has the maximum (100%).

4. SIMULATION RESULTS

In this work the proposed GDI DFF circuit has been implemented in180µm technology to compare the GDI design with a set of representative flip-flops, commonly used for high performance design. Nine sets of comparisons were carried out on the test circuits.

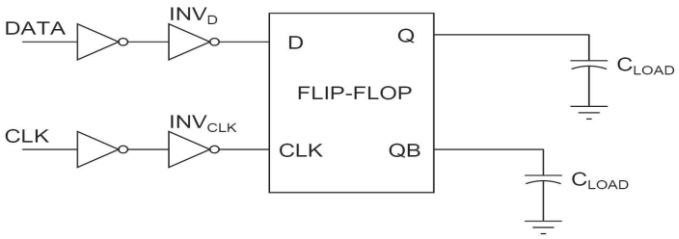

Figure 8: simulation test bench setup

The circuits were simulated using Cadence Spectre at 1.8V (for 180nm technologies), 250 MHz and 27°C, with load capacitance of 100fF. In our simulations the parasitic capacitances were taken into account. The simulation setup is shown in Fig.7. The device under test was placed between input buffers to account for the current consumption from the previous stage, and output buffers to emulate real environmental conditions.

Circuit	No. of transistors	Total width (um)	CLK Power (uW)	Internal power (uW)	Total power (uW)
XCFF	21	188.9	490.4	368.4	858.8
DDFF	18	103.7	302.1	246.67	548.77
PHFF	18	62.4	190.7	161.14	351.84

Table 2: Simulation result for 180nm technology.

The relative results are presented in Table 2 and for 0.18µm technologies. The best results in each compared category are emphasized. It can be seen, that GDI PHFF Output performs

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the other circuits in terms of power-delay product and total gates area in both technologies (including the inverted inputs). The improvement in power-delay product in GDI is up to 32% in 0.18µm technology.

5. CONCLUSIONS

A new implementation of high-performance Pulsed hybrid Flip-Flop (PHFF) using Gate-Diffusion-Input technique was presented. The proposed circuit has a simple structure, based on Master-Slave principle, and contains 18 transistors. An optimization procedure was developed for GDI PHFF, based on iterative transistor sizing, while targeting a minimal power-delay product. Performance comparison with other DFF design techniques was shown, with respect to gate area, number of devices, delay and power dissipation. A variety of circuits have been implemented in 180nm technologies to compare the proposed GDI structure with a set of representative flip-flops, commonly used for high performance design, showing an up-to 32%reduce in power-delay product and up to 43% reduction of gates area in GDI.

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